Batray II™

Celeron® / Pentium III®
Single Board Computer with
Video, SCSI, and Ethernet

User's Guide

095-20080-00 Rev. A

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Chapter 1 - Introduction

The BATRAY II is an all-in-one full-sized single board computer that is designed to fit a high performance Pentium III or Celeron based processor and compatible with high-end computer system applications using the PCI/ISA bus architecture. It is designed to keep pace with today's quickly changing environment and to remain compatible with hardware and software designed for the IBM PC/AT. The PCI bus supports two on board PCI devices – VGA and LAN. VARs, OEMs, and Systems Integrators will find this beneficial in building high performance systemms.

This single board computer can run with either an Intel Pentium III or Celeron processor, and support DIMM up to 1GB DRAM. The enhanced on-board PCI IDE interface can support 4 drives up to PIO mode 4 timing and Ultra DMA/33 synchronous mode feature. The on-board Super I/O Chipset integrates floppy controller, two serial ports, one FIR (Fast Infrared) port and one parallel port. Two high performance 16C550 compatible UARTs provide 16-byte send/receive FIFOs, and the multi-mode parallel port supports SPP/EPP/ECP function. Besides, two Universal Serial Bus ports provide high-speed data communication between peripherals and PC.

The PICMG standard makes the BATRAY II work with the legacy ISA, ISA/PCI or multi-slots PCI-bus backplane. The on-board 32-pin DIP socket supports M-system Disk-On-Chip Flash disk up to 144MB. Built-in Watch-dog Timer function monitors your system status. Two 6-pin Mini-DIN connectors are provided to connect PS/2 mouse and keyboard. The on-board Flash ROM is used to make the BIOS update easier. A standard P8 power connector is reserved to directly get more power for embedded applications, and the additional 5-pin shrouded connector is reserved for connecting keyboard interface on the backplane. The high precision Real Time Clock/calendar is built to support Y2K for accurate scheduling and storing configuration information. One 4-pin header is designed to support ATX power function. A CPU overheat protection feature will give user more security and stability. All of these features make the BATRAY II excellent in stand-alone applications.

Chapter 1 - Introduction

How to Use This Manual

The manual describes how to configure your BATRAY II system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : Introduction. presents what is included with this package and gives an overview of the product specifications and basic system architecture for this model of single board computer.

Chapter 2 : Hardware Configuration Setting. shows the definitions and locations of Jumpers and Connectors so that the system may be easily configured.

Chapter 3 : System Installation. describes how to properly mount the CPU and main memory, M-systems Flash disk, or optional flat panel display interface module, to get a safe installation and give a programming guide for the Watch Dog Timer function. In addition, it will introduce and show the driver installation procedure for the Graphics Controller.

Chapter 4 : BIOS Setup Information. specifies the meaning of each setup parameter and how to get advanced BIOS performance or update a new BIOS. In addition, a POST checkpoint list gives a trouble-shooting guide.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **I-Bus/Phoenix** may make supplements or changes in the products described in this document at any time.

What is Included With This Package

The BATRAY II package includes:

- One BATRAY II single board computer
- One Printer port cable kit
- One serial port cable to support two interfaces
- One FDC cable
- One IDE cable
- One 5-pin to 5-pin keyboard cable for backplane connection
- One 4-pin ATX power control cable for backplane connection
- One CD to support CHIPS B69000 VGA display driver and Intel 82559 LAN driver

If any of these items is damaged or missing, please contact your sales representative and save all packing materials for future replacement and maintenance.

Product Specifications

- **Main processor**
  - Intel Celeron processor or Intel Pentium III processor
  - CPU bus clock : 66/100 MHz
  - CPU core/bus clock ratio : x2 to x8
- **BIOS**
  - AMI system BIOS with 256KB Flash ROM to support DMI, PnP, APM,
  - and ACPI (option)
- **Main Memory**
  - Four 168-pin DIMM sockets, supporting 3.3V SDRAM with parity/ECC function
  - up to 1GB
- **L2 Cache Memory**
  - 128KB L2 cache built in Celeron and 256KB in Coppermine processor
- **Chipset**
  - Intel 440BX AGPset
- **Bus Interface**
  - Follow PICMG standard (32-bit PCI and 16-bit ISA bus)
  - Fully complies with PCI bus specification V2.1
- **PCI IDE Interface**
  - Support two enhanced IDE ports up to four HDD devices with PIO mode 4
  - and Ultra DMA/33 mode 2 timing transfer
- **Floppy Drive Interface**
  - Support one FDD port up to two floppy drives and 5-1/4”(360K, 1.2MB),
  - 3-1/2” (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD (option)
- **Serial Ports**
  - Support two high-speed 16C550 compatible UARTs with 16-byte T/R FIFOs

Product Specifications (continued)

- **IR Interface**
  - Support one 6-pin header for serial Fast/Standard Infrared wireless communication
- **Parallel Port**
  - Support SPP, Bi-direction, and EPP/ECP modes
- **USB Interface**
  - Support two USB (Universal Serial Bus) ports for high speed I/O peripheral devices
- **PS/2 Mouse and Keyboard Interface**
  - Support two 6-pin Mini-DIN connectors and one 5-pin shrouded connector for PS/2 mouse, keyboard and backplane connection
- **ATX Power Control Interface**
  - One 4-pin header to support ATX power control with Modem Ring-On and Wake-On-LAN function
- **Auxiliary I/O Interfaces**
  - System reset switch, external speaker, Keyboard lock and HDD LED interface
- **Real Time Clock/Calendar**
  - Support Y2K Real Time Clock/calendar with battery backup for 10-year data retention
- **Watchdog Timer**
  - 0.5,1,2,4,8,16,32,64 sec. time-out intervals by jumper setting or 255 intervals from 0.5 min. to 254.5 min. by software programming
- **DiskOnChip Feature**
  - Reserved one 32-pin socket for M-systems Flash Disk up to 144MB
- **On–board VGA Interface**
  - Adopt CHIPS 69000 HiQVideo Accelerator with integrated memory 2MB to provide high performance graphics and panel display capabilities

Product Specifications (continued)

- **On–board Ethernet**
  - Utilize Intel 82559 Fast Ethernet controller to support RJ-45 interface at 10/100BASE-T speed
- **CPU Overheat Protection**
  - Auto speed down when CPU overheats (OS independent & Driverless)
- **System Monitoring Feature**
  - Monitor CPU and system temperature, operating voltage, and fan status
- **Power Good**
  - On-board power good generator with reset time, 300ms ~ 500ms
- **Physical and Environmental Requirements**
  - Outline Dimension (L X W) : 338.5mm (13.36”) X 121.5mm (4.78”)
  - Board Weight : 0.92 lb. (0.42kg)
  - PCB layout : 6 layer
  - Power Requirements : +5V @6A (typ.), +12V @140mA, -12V @30mA
  - Operating Temperature : 0°C ~ 60°C (32°F ~ 140°F)
  - Storage Temperature : -20°C ~ 80°C
  - Relative Humidity : 5% ~ 95%, non-condensing

System Architecture

BATRAY II is a highly integrated system solution. The up-to-date system architecture of BATRAY II, includes two main VLSI chips, 82443BX Host Bridge and 82371EB PIIX4E, to support a Pentium III or Celeron processor, SDRAM with ECC, PCI bus interface, ACPI compliant power management (option), USB port, SMBus communication, and Ultra DMA/33 IDE Bus Master. The on-board super I/O chip , W83977ATF, will support PS/2 Keyboard/Mouse, two UARTs, FDC, Parallel and Infrared interface. In addition, an on-board PCI device VGA/panel display provides flexibility and reliability in a highly integrated application.

The built-in Socket 370 supports an Intel Celeron processor Plastic Pin Grid Array (PPGA**)** package or Pentium-III (FC-PGA) processor for a high performance and cost-effective application. The Intel Celeron processor, like the Intel Pentium Pro and Intel Pentium II processor, features a Dynamic Execution microarchitecture and also executes MMX technology instructions for enhanced media and communication performance. However, the Pentium III processor provides twice the Celeron L2 Cache.

The North Bridge 82443BX provides a completely integrated solution for the system controller and data path components in the system. It provides a 64-bit GTL+ based host bus interface, optimized 64-bit DRAM interface with ECC to support two 3.3V DIMMs at the maximum bus frequency of 100 MHz, and 32-bit PCI bus interface to support an on-board PCI device.

The South Bridge, 82371EB PCI ISA IDE Xcelerator (PIIX4E), provides a highly integrated multifunction PCI-to-ISA bridge solution. It supports 1-channel dedicated Ultra DMA-33 IDE master interface, full Plug-and-Play compatibility, and Advanced Programmable Interrupt Controller **(APIC)** interface on BATRAY II. It also supports 2-port Universal Serial Bus **(USB)** and PCI 2.1 Compliance operation. In addition, it also provides XD-bus via buffer logic control to support BIOS read/write access and external Real-time Clock **(RTC)** to maintain date and time of a system.

The Super I/O chip W83977ATF, integrates two high-speed serial ports, one parallel port, FIR/SIR interface, 8042 keyboard controller with PS/2 mouse ports and FDD interface. This parallel port supports one PC-compatible printer port (SPP), Enhanced Parallel Port **(EPP)** and Extended Capabilities Port **(ECP)**.

Chapter 1 - Introduction

The BATRAY II, contains a Watch-dog Timer **(WDT)** enabled by jumper setting and triggered by software, and a DiskOnChip **(DOC)** for M-systems Flash disk. An advanced feature of the BATRAY II is to support detection of the CPU temperature. The CPU operation will be automatically forced to slow down when overheating happens.

The graphics display port is a PCI device powered by the CHIPS 69000 graphics accelerator to support one VGA display and one panel interface port. The LAN port is a PCI device powered by Intel 82559 10/100 Ethernet Controller supporting Fast Ethernet interface through an RJ-45 connector.

All details of operating relationships are shown in Figure 1-1: BATRAY II System Block Diagram.

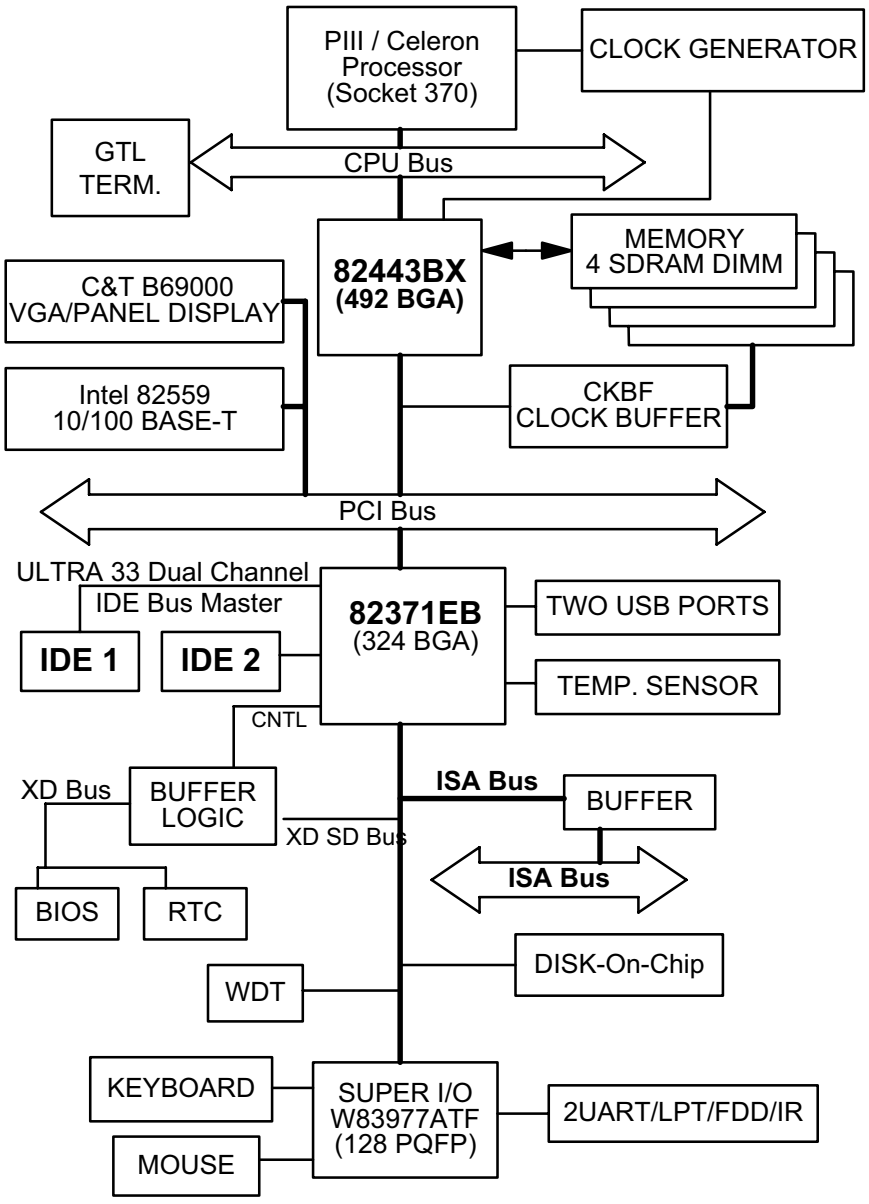

Figure 1-1: Batray II System Block Diagram

Chapter 2 - Hardware Configuration Setting

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on BATRAY II are in the correct position as shipped. The factory default settings are marked with an asterisk (*).

Jumpers

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. Others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (close) or remove (open) it from the jumper pins according to the following instructions.

(Refer to Figure 2-1 for jumper positions)

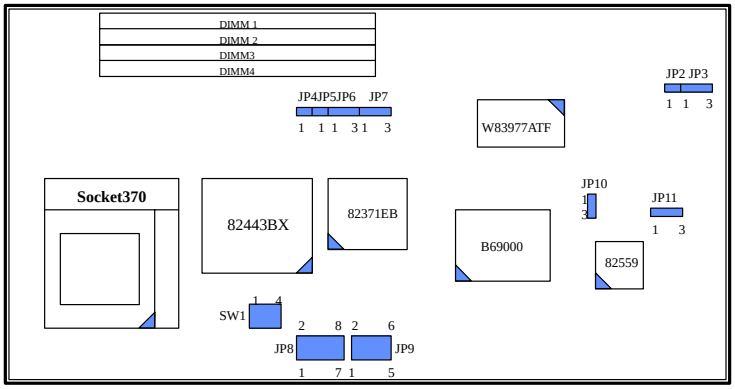

Figure 2-1: Batray II Jumper Locations

CPU Jumper Setting Table (SW1)

• **SW1** DIP switch settings for CPU core/bus ratio

SW-1	SW-2	SW-3	SW-4	CORE/BUS RATIO
OFF	OFF	ON	OFF	1.5x
OFF	OFF	OFF	OFF	2.0x
ON	ON	ON	ON	2.0x
ON	OFF	ON	ON	2.5x
ON	ON	OFF	ON	3.0x
ON	OFF	OFF	ON	3.5x
ON	ON	ON	OFF	4.0x
ON	OFF	ON	OFF	4.5x
ON	ON	OFF	OFF	5.0x
ON	OFF	OFF	OFF	5.5x*
OFF	ON	ON	ON	6.0x
OFF	OFF	ON	ON	6.5x
OFF	ON	OFF	ON	7.0x
OFF	OFF	OFF	ON	7.5x
OFF	ON	ON	OFF	8.0x
OFF	ON	OFF	OFF	Reserved

NOTE : For system stability, do not arbitrarily set CPU to run over speed unless you can handle BIOS parameters.

• Disk-On-Chip Jumper Setting (JP8)

1 – 2	3 – 4	5 – 6	7 – 8	Memory Address Window
Short	NC	NC	NC	D0000 – D1FFF*
NC	Short	NC	NC	D2000 – D3FFF
NC	NC	Short	NC	D4000 – D5FFF
NC	NC	NC	Short	D6000 – D7FFF

• Watch-Dog Timer Jumper Setting (JP4, JP5, JP6, JP7, JP9)

JP4 NC : Enabled WDT function
Short : Disabled WDT function *

JP5 NC : Allocate I/O port 0533H/0033H for programming of H/W WDT *
Short : Allocate I/O port 0543H/0343H for programming of H/W WDT

JP6 1 – 2 : Connect WDT output to system reset *
2 – 3 : Connect WDT output to NMI

JP9 WDT Time-out Interval (Twd) settings

5-6	3-4	1-2	Time-out Interval (Twd)
Short	Short	Short	0.5 sec.
Short	Short	NC	1 sec. *
Short	NC	Short	2 sec.
Short	NC	NC	4 sec.
NC	Short	Short	8 sec.
NC	Short	NC	16 sec.
NC	NC	Short	32 sec.
NC	NC	NC	64 sec.

JP7 WDT Time-out sources :

1 – 2 : initiated from hardware WDT by setting JP9 *
2 – 3 : initiated from software WDT by programming super I/O chipset W83977ATF

• RTC CMOS Clear Jumper Setting (JP2)

JP2 NC : Normal operation *
Short : Clear CMOS contents

NOTE: This CMOS clearing operation can be done under system power on if CMOS RAM CLEAR FUNCTION does not exist in Advanced Chipset Setup. It also can be done under system power on or off. However please make sure that the CMOS RAM clear option has been enabled in Advanced Chipset Setup before clearing CMOS.

• AT/ATX Power Supply Selection (JP3)

JP3	1 – 2 : Select ATX power supply 2 – 3 : Select AT power supply *

• Onboard devices (VGA/Ethernet) enable/disable jumper (JP10/JP11)

JP10	1 – 2 : Normal operation * 2 – 3 : Disable onboard VGA
JP11	1 – 2 : Normal operation * 2 – 3 : Disable onboard Ethernet

Connectors

I/O peripheral devices and Flash disk will be connected to these interface connectors or DOC socket located on this single board computer.

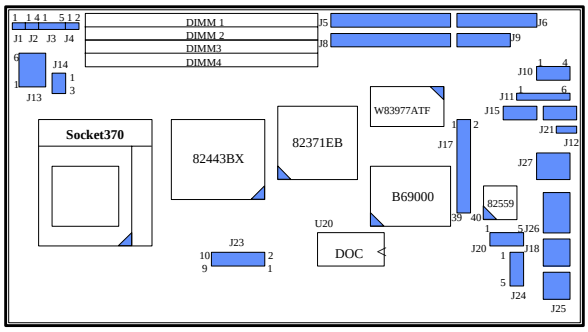

Figure 2-2: Batray II Connector Locations

CONNECTOR	FUNCTION	REMARK
J1	System reset	
J2	External speaker interface	
J3	Keyboard lock and power indicator	
J4	IDE active LED interface	
J5	IDE1 (Primary) interface	
J6	Floppy connector	
J8	IDE2 (Secondary) interface	
J9	Parallel port connector	
J10	ATX power control interface	Connect to Backplane
J11	IrDA (infrared) port	Support FIR/SIR
J12	ATX power button interface	Connect to Chassis
J13	Standard P8 power connector	
J14	CPU cooling fan power connector	Support +12V
J15	COM1 serial port	2 x 5 shrouded
J17	Flat Panel display module interface	2x20 pin header
J18	PS/2 mouse connector	6-pin Mini-DIN
J20	External PS/2 mouse connector	Connect mouse cable kit
J21	COM2 serial port	2 x 5 shrouded
J23	External USB interface	Support two ports
J24	External keyboard interface	Connect to backplane
J25	PS/2 keyboard connector	6-pin Mini-DIN
J26	VGA connector	DSUB-15
J27	Ethernet connector	RJ-45
U20	On-board Flash disk (DiskOnChip)	32-pin DIP socket

Pin Assignments of Connectors

• J1 : Reset Header

PIN No.	Signal Description
1	Reset
2	Ground

• J2 : External Speaker Header

PIN No.	Signal Description
1	Speaker signal
2	N/C
3	Ground
4	+5V

• J3 : Keyboard Lock Header

PIN No.	Signal Description
1	+5V (330 ohm pull-up for power LED)
2	N/C
3	Ground
4	Keyboard inhibit
5	Ground

• J4 : IDE1 Active LED Header

PIN No.	Signal Description
1	+5V (470 ohm pull-up for HDD LED)
2	HDD Active # (LED cathode terminal)

• J10 : ATX Power Control Connector

PIN No.	Signal Description
1	ATX Power Good Signal
2	ATX 5V Stand-by
3	ATX Power On Control
4	Ground

• J5/ J8 : IDE1/IDE2 Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	N/C
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD Active#	40	Ground

• J11 : Fast & Standard IrDA Header

PIN No.	Signal Description
1	VCC (+5V)
2	FIRRX
3	SIRRX
4	Ground
5	IRTX
6	N/C

• J14 : CPU Cooling FAN Power Connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Pull-up +5V (Reserved for fan sense)

• J6 : FDC Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select
3	Ground	4	N/C
5	Ground	6	N/C
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor ENB#
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Head Select#
33	Ground	34	Disk Change#

• J9 : Parallel Port Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	14	Auto Form Feed#
2	Data 0	15	Error#
3	Data 1	16	Initialization#
4	Data 2	17	Printer Select IN#
5	Data 3	18	Ground
6	Data 4	19	Ground
7	Data 5	20	Ground
8	Data 6	21	Ground
9	Data 7	22	Ground
10	Acknowledge#	23	Ground
11	Busy	24	Ground
12	Paper Empty	25	Ground
13	Printer Select	26	N/C

• J13 : Standard P8 Power Connector

PIN No.	Signal Description
1	N/C
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

• ¦ J18 : PS/2 Mouse Connector (6-pin Mini-DIN)

PIN No.	Signal Description
1	Mouse Data
2	N/C
3	Ground
4	+5V
5	Mouse Clock
6	N/C

• J20 : External PS/2 Mouse Connector

PIN No.	Signal Description
1	Mouse Clock
2	Mouse Data
3	N/C
4	Ground
5	+5V

• J23 : External USB Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	N/C
3	SBD0- (USBP0-)	4	Ground
5	SBD0+ (USBP0+)	6	SBD1+ (USBP1+)
7	Ground	8	SBD1- (USBP1-)
9	N/C	10	+5V

• J12 : ATX Power Button Interface

PIN No.	Signal Description
1	Power Button Control Signal
2	Ground

• J17 : Flat Panel Display Module Interface

PIN No.	Signal Description	PIN No.	Signal Description
1	P0	2	P1
3	P2	4	P3
5	P4	6	P5
7	P6	8	P7
9	P8	10	P9
11	P10	12	P11
13	P12	14	P13
15	P14	16	P15
17	Ground	18	P16
19	SHFCLK	20	P17
21	Ground	22	Ground
23	P18	24	P19
25	P20	26	P21
27	P22	28	P23
29	FLM	30	ENAVEE
31	LP	32	PCLK
33	M	34	+5V
35	+12V	36	+5V
37	+12V	38	+5V
39	Ground	40	Ground

• J24 : External Keyboard Connector

PIN No.	Signal Description
1	Keyboard Clock
2	Keyboard Data
3	N/C
4	Ground
5	+5V

• J25 : PS/2 Keyboard Connector (6-pin Mini-DIN)

PIN No.	Signal Description
1	Keyboard Data
2	N/C
3	GND
4	+5V
5	Keyboard Clock
6	N/C

• J27: Ethernet RJ-45 Interface Connector

PIN No.	Signal Description
1	TX+
2	TX-
3	RX+
4	Termination to Ground
5	Termination to Ground
6	RX-
7	Termination to Ground
8	Termination to Ground

• J15/J21 : Serial Port 2x5 Shrouded Connector

PIN	Signal Description	PIN	Signal Description
1	Data Carrier Detect (DCD)	6	Data Set Ready (DSR)
2	Receive Data (RXD)	7	Request to Send (RTS)
3	Transmit Data (TXD)	8	Clear to Send (CTS)
4	Data Terminal Ready (DTR)	9	Ring Indicator (RI)
5	Ground (GND)	10	N/C

• J26 : VGA DSUB-15 Connector

PIN No.	Signal Description
1	R
2	G
3	B
4	N/C
5	Ground
6	Ground
7	Ground
8	Ground
9	N/C
10	Ground
11	N/C
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Chapter 3 - System Installation

This chapter provides instructions on setting up your system. Additional information is given to show how to install the M-systems Flash disk, set up LCD display, and handle WDT operation in software program.

Socket 370 Celeron/Pentium III Processor

Installing CPU

1. Lift the handling lever of CPU socket outwards and upwards to the other end.
2. Align the processor pins with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. Instead, check and align the CPU pins uniformly.
3. Push down the lever to lock processor chip into the socket.
4. Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 370.
5. Be sure to pay attention to the CPU speed and voltage type to adjust the jumper settings properly.

Removing CPU

1. Unlock the cooling fan first.
2. Lift the lever of CPU socket outwards and upwards to the other end.
3. Carefully lift up the existing CPU to remove it from the socket.
4. Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

Chapter 3 - System Installation

Main Memory

BATRAY II provides four 168-pin Dual In-line Memory Modules **(DIMM)** to support on-board main memory. The maximum memory size for 3.3V EDO DRAM or SDRAM is 1GB. Normally, the DIMM used could be either 3.3V EDO (Extended Data Out) memory with speed less than 70ns or 3.3V SDRAM (Synchronized DRAM) with speed less than 100ns (-10). If you adopt 100MHz system clock, you need to use SDRAM with speed less than 80ns (-8). It is better to use a PC100-compliant memory chip on your system.

For system compatibility and stability, do not use a “no-name” memory module. You can use either the single or double-side DIMM without parity check and ECC function.

Insure that the memory modules are properly seated and locked in place. Failing to do so will affect system reliability. Follow the normal procedure to install the DRAM module into the memory socket. Before locking, make sure that the module has been fully inserted into card slot.

NOTE:

For maintaining system stability, don’t change any of DRAM parameters in BIOS setup without acquiring all pertinent technical information.

M-systems Flash Disk

BATRAY II reserves one 32-pin DIP socket for installing M-systems Flash disk from 2MB to 144MB. This operation structure is running with pure ISA-bus without PnP (Plug and Play) function. Before installing, be sure that the I/O address jumper is set on the correct position to prevent a resource conflict causing an unworkable system. Also, remember to follow the prescribed DOC (DiskOnChip) installation procedure. Otherwise, the Flash chip may be burned out.

Installing DOC

Align the DOC with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of DOC corresponds to notched corner of the socket. Then press the DOC gently until it fits into place. If installation procedure is correct, the Flash disk can be viewed as a normal hard disk to access read/write data.

WARNING:

Please ensure that the DOC is properly inserted. Installing the DOC incorrectly will cause severe damage to it.

If you want to boot from this Flash disk, it is necessary to refer to the application note from M-systems. The necessary information may be found in the M-Systems product manual or on their web site **http://www.m-sys.com**.

Installing the Single Board Computer

Perform the following steps to install the BATRAY II into a standard chassis or proprietary environment:

1. Check that all jumper setting are correct.
2. Install and configure CPU and memory module in the correct position
3. Place the BATRAY II into the dedicated position in your system
4. Attach cables to existing peripheral devices and secure it

CHIPS 69000 Graphics Controller

The following table shows how to enable and disable the on-board C&T 69000 VGA function.

JP10	FUNCTION
1-2	Enable on-board VGA
2-3	Disable on-board VGA

The on-board graphics controller adopts CHIPS 69000 that integrates high performance memory technology for the graphics frame buffer. Based on the proven HiQVideo graphics accelerator core, the 69000 combines state-of-the-art flat panel controller capabilities with low power, high performance integrated memory. It incorporates 2MB of proprietary integrated SDRAM for the graphics/video frame buffer. The integrated SDRAM memory can support up to 83MHz operation, thus increasing the available memory bandwidth for the graphics subsystem to support high color/high resolution application.

The 69000 supports a wide variety of monochrome and color Single-Panel, Single-Drive and Dual-Panel, Dual Drive, standard and high-resolution, passive STN and active matrix TFT/MIM LCD, and EL panels. It is designed to support high performance graphics and video acceleration for all supported display resolutions, display types, and color modes. This 69000 PCI device can be configured to operate an analog CRT monitor and flat panel at the same time.

Display Modes Supported

The 69000 supports the display modes shown in the table below.

Resolution	Color (bpp)	Refresh Rates (Hz)
640x480	8	60, 75, 85
640x480	16	60, 75, 85
640x480	24	60, 75, 85
800x600	8	60, 75, 85
800x600	16	60, 75, 85
800x600	24	60, 75, 85
1024x768	8	60, 75, 85
1024x768	16	60, 75, 85
1280x1024	8	60

BATRAY II utilizes on-board CHIPS 69000 and optional panel display module to support 16 types of panels. You can select one of sixteen LCD panel types by BIOS panel setting in Advanced CMOS Setup.

LCD Panel Interface Kit

The BATRAY II provides one flat panel interface connector J17 (see Chapter 2) to connect the panel interface kit for VGA, SVGA and XGA panel support. This installation is very simple,requiring no special tools. Simply do the board-to-board connection and lock up the screw. The LCD-INTR-ROBO is an optional kit that provides an interface between BATRAY II and LCD-kit which is connected to LCD modules.

LCD-INTR-ROBO

There are two types of LCD-Kits available for BATRAY II panel application.

* LCD-KIT-RS optional kit for TFT SVGA LCD panel

* LCD-KIT-RX optional kit for XGA LCD panel

Driver Support

BATRAY II provides one CD to support on-board VGA device drivers in various operating systems. This CD only includes one directory **\vga69000**. Before installing the device driver, please see the reference files in each sub-directory. **You can not install driver from CD directly.**

vga69000 : supports NT3.5, NT4.0, WIN95 and Win98 environment.

Important Notice !

For the successful installation of VGA driver in NT3.51 environment, create a diskette named "Disk 1" with the VGA drivers to support valid data path. Prepare one diskette and create a directory, \disk 1, under its root. Copy all files under \vga69000\NT_35 from the CD-Title into \disk 1. When the computer asks for VGA drivers during the installation of NT3.51, the VGA drivers will all be located in the diskette, Disk 1.

Intel 82559 Fast Ethernet Controller

The following table shows the jumper positions to enable and disable the on-board Intel 82559 LAN function,

JP11	FUNCTION
1-2	Enable on-board LAN
2-3	Disable on-board LAN

Drivers Support

Please find 82559 LAN driver in Ethernet directory of BATRAY II CD.

On-board LED Indicator

The BATRAY II provides three LED indicators to show LAN interface status. These messages will give you a guide for troubleshooting.

LED1 (top) (LAN speed LED)

ON : indicates 100Mbps activity
OFF : indicates 10Mbps activity

LED2 (center) (LAN active LED)

ON : indicates Tx/Rx activity
OFF : no activity

LED3 (bottom) (LAN Link Integrity LED)

ON : indicates link is good in either 10 or 100 Mbps
OFF : link is bad

Watch Dog Timer Programming

There are two options to activate the Watch-Dog Timer (WDT) function. One is to utilize hardware jumper setting and program by software command. After this feature is enabled, a system reset will be generated unless a application triggers the timer periodically within time-out period. This allows the system to restart in an orderly way in case any abnormal condition is found.

A second option is to program super I/O W83977ATF chip to start WDT time-out counting. The first option is recommended because the second is comparatively difficult and complicated. In addition, you can also connect WDT output to NMI input by setting JP6 jumper to generate NMI event to support special interrupt service routine.

An optional two-port WDT is provided on BATRAY II. This WDT comes with 8 possible ranges of time intervals from 500 ms to 64 sec., which can be adjusted by setting jumper positions. It could be enabled and programmed by reading I/O port 0533H or 0543H to issue trigger continuously, and disabled by reading I/O port 0033H or 0343H. A tolerance of 30% timer limit must be considered. For instance, if the time-out interval is set to 1second, the WDT trigger command must be issued within 700ms at least.

The example below gives you a sample algorithm for WDT programming via I/O port 0533H and 0033H in your application program :

Enable WDT

```
MOV     DX, 0533H
IN      AL, DX
```

Re-trigger WDT

```
MOV     DX, 0533H
IN      AL, DX
```

Disable WDT

```
MOV     DX, 0033H
IN      AL, DX
```

NOTE

Please contact technical support to get WDT programming information on super I/O chip W83977ATF for long time-out interval support from 0.5 minutes to 254.5 minutes.

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Chapter 4 - BIOS Setup Information

BATRAY II is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in setup program that allows users to easily modify the basic system configuration. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When the system is turned on, BATRAY II communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors may be significant enough to abort the start-up.

Entering Setup

To enter the BIOS Setup program

1. Turn on or reboot the computer.
2. Press the <Del> key immediately to enter the BIOS setup program when the message “Hit <del> if you want to run setup” appears.

If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and then ON, or by pushing the “RESET” button. You may also restart by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys simultaneously, the system will not boot and an error message will be displayed, asking you to:

Press <F1> to run SETUP or Resume.

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below shows the keystroke functions in BIOS setup.

EDITING KEYS	FUNCTION
<Tab>	Move to the next field
← ↑ → ↓	Move the next field to the left, above, right, or below
<Enter>	Select in the current field
+ /–	Increments / Decrements a value
<Esc>	Close the current operation and return to previous level
<PgUp>	Returns to the previous option
<PgDn>	Advances to the next option
<F2>/<F3>	Select background color
<F10>	Show “Save current settings and exit (Y/N)” in main menu

Chapter 4 - BIOS Setup Information

Main Menu

Once in the BATRAY II AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from eleven setup functions and two exit choices. Use arrow keys to switch the items and press <Enter> key to accept or enter the sub-menu.

.

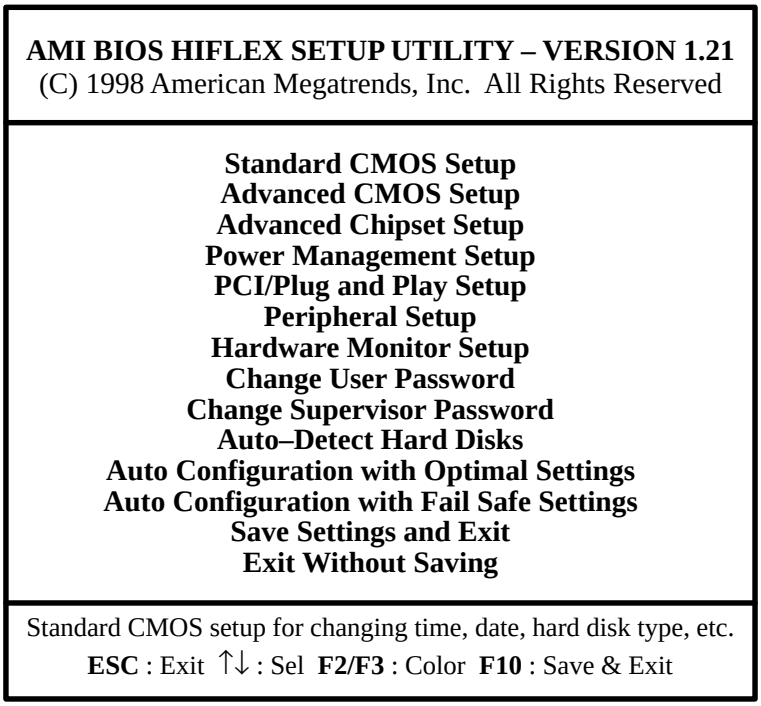

Figure 4-1: Main Menu Screen

NOTE

It is strongly recommended to reload Optimal Setting if CMOS is lost or BIOS is updated.

CMOS Setup Reference Table

The setup reference table includes all the Optimal, Fail-safe, and Other options setting in each BIOS setup item. If more detail is needed, refer to the item description in the sub-sections.

ADVANCED CMOS SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
Quick Boot	Enabled	Enabled	
1st Boot Device	IDE-0	IDE-0	IDE-1, IDE-2, IDE-3, Floppy, CD-ROM, ATAPI ZIP, LS-120, SCSI, Network
2nd Boot Device	Floppy	Floppy	IDE-1, CD-ROM
3rd Boot Device	ATAPI ZIP	ATAPI ZIP	IDE-1, ATAPI ZIP
4th Boot Device	Disabled	Disabled	IDE-1, CD-ROM
Try Other Boot Device	Yes	Yes	No
S.M.A.R.T. for Hard Disks	Disabled	Disabled	Enabled
BootUp Num-Lock	On	On	Off
PS/2 Mouse Support	Enabled	Enabled	Disabled
System Keyboard	Absent	Absent	Present
Primary Display	Absent	Absent	VGA/EGA, Mono
Password Check	Setup	Setup	Always
Boot To OS/2 > 64MB	No	No	Yes
System BIOS Cacheable	Enabled	Disabled	
C000, 16K Shadow	Cached	Cached	Enabled, Disabled
C400, 16K Shadow	Cached	Cached	Enabled, Disabled
C800, 16K Shadow	Cached	Cached	Enabled, Disabled
CC00, 16K Shadow	Disabled	Disabled	Cached, Enabled
D000, 16K Shadow	Disabled	Disabled	Cached, Enabled
D400, 16K Shadow	Disabled	Disabled	Cached, Enabled
D800, 16K Shadow	Disabled	Disabled	Cached, Enabled
DC00, 16K Shadow	Disabled	Disabled	Cached, Enabled

ADVANCED CHIPSET SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
Configure SDRAM Timing by SPD	Disabled	Disabled	Enabled
SDRAM RAS# to CAS# delay	3 SCLKs	3 SCLKs	2 SCLKs
SDRAM RAS# Precharge	3 SCLKs	3 SCLKs	2 SCLKs
SDRAM CAS# Latency	3 SCLKs	3 SCLKs	2 SCLKs
SDRAM Lead off Cmd Timing	Auto	Auto	4 SCLKs, 3 SCLKs
DRAM Integrity Mode	Non-ECC	Non-ECC	EC-Only, ECC H/W
DRAM Refresh Rate	15.6 us	15.6 us	31.2 us, 62.4 us, 124.8 us, 249.6 us
Memory Hole	Disabled	Disabled	512KB-640KB, 15MB-16MB
8bit I/O Recovery Time	1 Sysclk	1 Sysclk	Disabled, 2, 3, 4, 5, 6, 7, 8 Sysclk
16bit I/O Recovery Time	1 Sysclk	1 Sysclk	Disabled,2,3,4 Sysclk
USB Passive Release	Enabled	Enabled	Disabled
PIIX4 Passive Release	Enabled	Enabled	Disabled
PIIX4 Delayed Transaction	Disabled	Disabled	Enabled
Spread Spectrum Control	Disabled	Disabled	Enabled
USB Function	Disabled	Disabled	Enabled
USB Keyboard Legacy Support	Enabled	Enabled	Disabled
CMOS RAM CLEAR FUNCTION	Disabled	Disabled	Enabled
LCD CRT Selection	CRT Only	CRT Only	Simultaneous, LCD Only
LCD Type	Type 7	Type 7	Type 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, 16

POWER MANAGEMENT SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
Power Management / APM	Enabled	Disabled	
Green PC Monitor Power State	Off	Off	Stand By, Suspend
Video Power Down Mode	Disabled	Disabled	Stand By, Suspend
Hard Disk Power Down Mode	Disabled	Disabled	Stand By, Suspend
Standby Time Out (Minute)	Disabled	Disabled	1, 2, 4, 8, 10, 20, 30, 40, 50, 60 Min.
Suspend Time Out (Minute)	Disabled	Disabled	1, 2, 4, 8, 10, 20, 30, 40, 50, 60 Min.
Throttle Slow Clock Ratio	50 – 62.5%	50 – 62.5%	0-12.5%, 12.5-25%, 25-37.5%, 37.5-50%, 62.5-75%, 75-87.5%
Display Activity	Ignore	Ignore	Monitor
Device 6 (Serial Port 1)	Monitor	Monitor	Ignore
Device 7 (Serial Port 2)	Monitor	Monitor	Ignore
Device 8 (Parallel Port)	Ignore	Ignore	Monitor
Device 5 (Floppy disk)	Monitor	Monitor	Ignore
Device 0 (Primary master IDE)	Monitor	Monitor	Ignore
Device 1 (Primary slave IDE)	Ignore	Ignore	Monitor
Device 2 (Secondary Master IDE)	Monitor	Monitor	Ignore
Device 3 (Secondary slave IDE)	Ignore	Ignore	Monitor
System Thermal	Ignore	Ignore	Monitor
Thermal Slow Clock Ratio	50 – 62.5%	50 – 62.5%	0 – 12.5%, 12.5 – 25%, 25 – 37.5%, 37.5 – 50%, 62.5 – 75%

POWER MANAGEMENT SETUP DEFAULTS (Continued)

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
CPU Critical Temperature	75?/167?	75?/167?	Disabled, 45°C/113°F, 50°C?/122°F?, 55°C?/131°F?, 60°C?/140°F?, 65°C?/149°F?, 70°C?/158°F? 75°C/167°F
Power Button Function	On/Off	On/Off	Suspend
Ring Resume From Soft Off	Disabled	Disabled	Enabled

PCI / PnP SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
Plug and Play Aware O/S	No	No	Yes
Clear NVRAM	No	No	Yes
PCI Latency Timer (PCI Clocks)	64	64	32, 96, 128, 160, 192, 224, 248
PCI VGA Palette Snoop	Disabled	Disabled	Enabled
Allocate IRQ to PCI VGA	Yes	Yes	No
PCI IDE BusMaster	Disabled	Disabled	Enabled
OffBoard PCI IDE Card	Auto	Auto	Slot1, Slot2, Slot3, Slot4
OffBoard PCI IDE Primary IRQ	Disabled	Disabled	INTA, INTB, INTC, INTD, Hardwired
OffBoard PCI IDE Secondary IRQ	Disabled	Disabled	INTA, INTB, INTC, INTD, Hardwired
PCI Slot1 IRQ Priority	Auto	Auto	3, 4, 5, 7, 9, 10, 11
PCI Slot2 IRQ Priority	Auto	Auto	3, 4, 5, 7, 9, 10, 11
PCI Slot3 IRQ Priority	Auto	Auto	3, 4, 5, 7, 9, 10, 11

PCI / PnP SETUP DEFAULTS (Continued)

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
PCI Slot4 IRQ Priority	Auto	Auto	3, 4, 5, 7, 9, 10, 11
DMA Channel 0	PnP	Pnp	ISA/ EISA
DMA Channel 1	PnP	Pnp	ISA/ EISA
DMA Channel 3	PnP	Pnp	ISA/ EISA
DMA Channel 5	PnP	Pnp	ISA/ EISA
DMA Channel 6	PnP	Pnp	ISA/ EISA
DMA Channel 7	PnP	Pnp	ISA/ EISA
IRQ3	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ4	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ5	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ7	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ9	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ10	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ11	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ12	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ14	PCI/ PnP	PCI/ PnP	ISA/ EISA
IRQ15	PCI/ PnP	PCI/ PnP	ISA/ EISA

PERIPHERAL SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Fail-safe Default	Other Options
On board FDC	Auto	Auto	Enabled, Disabled
On board Serial Port A	Auto	Auto	3F8h/COM1, 2F8h/COM2, 3E8h/COM3, 2E8h/COM4, Disabled
On board Serial Port B	Auto	Auto	3F8h/COM1, 2F8h/COM2, 3E8h/COM3, 2E8h/COM4, Disabled
On board IR Port	Disabled	Disabled	3F8h/COM1, 2F8h/COM2, 3E8h/COM3, 2E8h/COM4, Auto
IR Mode Select	N/A	N/A	IrDA, ASK-IR, FIR
IR IRQ Select	N/A	N/A	3, 4, 5, 9, 10, 11, 12
IR DMA Select	N/A	N/A	0, 1, 3
On board Parallel Port	Auto	Auto	Disabled, 378h, 278h, 3BCh
Parallel Port Mode	Bi-Dir	Bi-Dir	EPP, ECP, Normal
EPP Version	N/A	N/A	1.7 , 1.9
Parallel Port IRQ	Auto	Auto	5, 7
Parallel Port DMA Channel	N/A	N/A	0, 1, 3
On board IDE	Both	Both	Disabled, Primary, Secondary

Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp> / <PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it. Follow command keys in CMOS Setup table to change **Date**, **Time**, **Drive type**, and **Boot Sector Virus Protection Status**.

Advanced CMOS Setup Menu

This setup includes all of the advanced features in the system. The detailed descriptions are specified below.

Quick Boot

Set “Disabled” for normal booting or select “Enabled” to skip minor BIOS test items to obtain quick boot response.

Boot Up Sequence

This category includes six items to determine which drive the computer searches first for the Disk Operating System (DOS).

The default ARMD (ATAPI Removable Media Device) emulation type is set to popular drive type LS-120 and ATAPI ZIP. The boot up device choices are: “Disabled”, “IDE-0”, “IDE-1”, “IDE-2”, “IDE-3”, “Floppy”, “LS-120”, “ATAPI ZIP”, “CD-ROM”, “SCSI”, or “NETWORK”.

Boot Up Num-Lock

Select “On” to enable numeric function of the numeric keypad, or “Off” to disable it.

PS/2 Mouse Support

Select “Enabled” to enable PS/2 mouse function, or “Disabled” to release IRQ12 interrupt for other ISA-bus I/O devices.

System Keyboard

This option will be used to neglect “keyboard error” when you choose the *Absent* setting in your BIOS setup and system has no keyboard attached.

Primary Display

Chooses *Absent*, *VGA/EGA, CGA40x25, CGA80x25,* or *Mono* to conform to your monitor type. If you select *Absent*, the "CMOS Display Type Wrong" message will be ignored regardless the mismatched display card.

Password Check

This option enables password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password.

Setup: If the current user's password is already entered in "Change User Password," this option will force the system to check the password before running setup.

Always : Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

Boot To OS/2 > 64MB

Choose "Yes" to support OS/2 environment.

System BIOS Cacheable

With this option enabled, system performance is enhanced by shadowing and caching system BIOS. When disabled, this BIOS shadow function will be ignored. The default option is "enabled."

Video BIOS Shadow

Select "Cached" option to get higher display performance by shadowing and caching VGA BIOS. If user chooses "Enabled" option, only BIOS shadow function is active. The "Disabled" option will ignore this BIOS caching and shadowing function.

Shadow Memory (from address C000 – DFFF, 16K per segment)

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. In general, C000 and C800 will be allocated for VGA BIOS and set to *Cached* to get higher display performance by shadowing and caching the feature. If the *Enabled* setting is chosen, only the BIOS shadow function is active.

Advanced Chipset Setup Menu

This setup is very important in maintaining system stability. If you are not technically knowledgeable, do not attempt to change any parameters. Choose the optimal default setting.

Configure SDRAM Timing by SPD

This option provides DIMM plug-and-play support by Serial Presence Detect (SPD) mechanism via the System Management Bus (SM Bus) interface. This option can be disabled to manage the following four SDRAM timing options manually. In addition, the SDRAM operating timing may follow a serial presence from EEPROM content by setting this option to “Enabled”, and all SDRAM timing options will be unavailable and hidden.

SDRAM RAS# to CAS# delay

This option controls the number of SCLKs (SDRAM Clock) from a row activated command to a read or write command. If the system has a good quality SDRAM, this option can be set to “2 SCLKs” to obtain better memory performance. Normally, the option will be set to *3 SCLKs*.

SDRAM RAS# Precharge

This option controls the number of SCLKs for RAS# precharge. If your system installs good quality of SDRAM, this option can be set to “2 SCLKs” to obtain better memory performance.

SDRAM CAS# Latency

This option controls the number of SCLKs between the time a read command is sampled by the SDRAMs and the time the North Bridge, 82443BX, samples correspondent data from the SDRAMs. For a registered DIMM with CAS# Latency = 2, this option should be set to “2 SCLKs” to acquire better memory performance.

SDRAM Lead off Cmd Timing

This option is used to control when the SDRAM command pins (SRASx#, SCASx# and Wex#) and CSx# are considered valid on lead offs for CPU cycles. If you select *Auto*, this timing will be automatically initialized and set by BIOS from CPU speed detection. For Desktop platforms, it might be set to 4 SCLKs. In general, another option *3 SCLKs* will be set to meet Mobile platforms.

DRAM Integrity Mode

There are three options *Non-ECC*, *EC-Only* (Error Check Only) and *ECC* Hardware (Error Checking and Correction) in this feature. The DRAM integrity mode will be implemented by the parity algorithm when this option is set to “Non-ECC”.

DRAM Refresh Rate

This option specifies the refresh rate frequency for the installed system memory SDRAM DIMMs. If you have good quality of DRAM, you can choose longer refresh rate to get better system performance.

Memory Hole

This option allows the end user to specify the location of a memory hole for memory space requirement from ISA-bus cards.

8-bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 8-bit I/O operations.

16-bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 16-bit I/O operations.

USB Passive Release

When enabled, PIIX4 is allowed to use Passive Release to obtain better USB performance while transferring control information or data for USB transactions. When disabled, PIIX4 will perform PCI accesses for USB without using Passive Release.

PIIX4 Passive Release

Choose the “Enabled” option to help raise the available bandwidth of the PCI bus for acquiring higher PCI bus performance.

PIIX4 Delayed Transaction

Choose the “Enabled” option to obtain higher PCI bus performance for I/O controller and bridge in the system.

Spread Spectrum Control

This option is for EMI test issue only.

USB Function

This option will enable the on-chip USB function to support USB (Universal Serial Bus) peripheral devices if the “Enabled” setting is chosen.

USB Keyboard Legacy Support

This feature will be automatically disabled and hidden if user chooses the “Disabled” setting from the foregoing USB Function option. Otherwise, enabling this option provides support for USB-keyboard without auxiliary driver under DOS environment.

CMOS RAM CLEAR FUNCTION

If your system supports Y2K RTC, set this option to *Enabled* to support hardware CMOS clearing operation.

LCD CRT Selection

There are three options, “CRT Only”, “LCD Only”, and “Simultaneous,” used to support display function. If you want to obtain better display quality and flexible refresh rate, you can choose “CRT Only” option. The default setting is *CRT Only*.

LCD Type

There are sixteen options from “Type 1” to “Type 16” for supporting the LCD panel display function. The final Panel Type will be decided by CMOS setting. The supported resolution is shown in the following table, The default setting is *Panel Type 7*.

Type	Flat Panel Type
1	1024x768 Dual Scan STN Color Panel àreserved
2	1280x1024 TFT Color Panel àreserved
3	640x480 Dual Scan STN Color Panel àreserved
4	800x600 Dual Scan STN Color Panel àreserved
5	640x480 Sharp TFT Color Panel àreserved
6	640x480 18-bit TFT Color Panel
7	1024x768 TFT Color Panel
8	800x600 TFT Color Panel
9	800x600 TFT Color Panel (L. BIOS) àreserved
10	800x600 TFT Color Panel (L. BIOS)
11	800x600 Dual Scan STN Color Panel (L. BIOS) àreserved
12	800x600 Dual Scan STN Color Panel (L. BIOS) àreserved
13	1024x768 TFT Color Panel (L. BIOS) àreserved
14	1280x1024 Dual Scan STN Color Panel (L. BIOS)àreserved
15	1024x600 Dual Scan STN Color Panel (L. BIOS) àreserved
16	1024x600 TFT Color Panel (Large BIOS)

Power Management Setup Menu

This APM (Advanced Power Management) determines how much power energy can be saved by setting the following items to handle system power resource. The following descriptions specify the definition of each item in detail.

Power Management/APM

This feature controls system power resources. Set this option to “Enabled” to enable the power management function.

Green PC Monitor Power State

This option is used to decide what kind of power states are effective. There are three options -- “Stand By”, “Suspend”, and “Off” -- in this feature. The “Stand By” option turns off light power by the handling of Monitor signals; the “Suspend” mode turns off heavy power; and the “Off” state turns off the power of the monitor.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after a specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management state that the HDD enters after a specified period of hard drive inactivity. It is the same as video power control. If “Stand By” or “Suspend” is chosen, it will depend on the parameter “Stand By Time out”or “Suspend Time out”.

Stand by Time out (Minute)

This option specifies the length of system inactivity with the computer in Full-On power state before the computer is placed in Standby mode. In Standby mode, some power use is curtailed.

Suspend Time out (Minute)

This option is the same as **Stand by Time out** function. These two features will be enabled to monitor power of sub-items “Display Activity”, “Serial port”, “Parallel Port”, “Floppy”, “Pri-HDD”, and “Sec-HDD” independently. It is also used to control CPU throttle running function. All of the sub-items will be ineffective in selection of disabling “Stand by Time out” or “Suspend Time out” even if it can be chosen by user in BIOS setup menu.

Throttle Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode.

Display Activity

This option specifies if BIOS is to monitor activity on the display monitor for power conservation purposes. If set to *Monitor* and the computer is in a power saving state, BIOS watches for video display activity. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend time out timers if activity occurs on the specified IRQ lines. If set to *Ignore*, video display monitor activity is not monitored.

Device 6/7/8/5/0/1/2/3 (Serial 1&2, Parallel, FDD, Pri/Sec HDD)

When set to *Monitor*, these options enable event monitoring on the specified hardware device. If set to *Monitor* and the computer is in a power saving state, BIOS watches for activity on the device with specified IRQ line. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend time out timers if activity occurs on the specified device. No monitoring activity occurs if the option is set to *Ignore*. The settings for each of these options are *Monitor* or *Ignore.*

System Thermal

Set this option to *Monitor* for CPU thermal monitoring and speed down control. The system will automatically supervise the CPU environmental temperature. If the CPU surface temperature reaches the trip point set in Hardware Monitor Setup, the thermal detection will be effective and CPU will run in throttle control manner. The overall system performance will be reduced to half. This option is a trade-off of system performance and stability and is configurable by user. The default setting is *Ignore*. You can choose *Monitor* setting to enable this thermal function.

Thermal Slow Clock Ratio

This option specifies the speed at which the system clock runs in thermal trip point. The settings are expressed as the duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the over heat mode.

CPU Critical Temperature

Set this option to monitor CPU thermal trip point defined by user. If the System Thermal option in CMOS setup is set to “Monitor” state and CPU surface temperature is over this critical temperature, the system will automatically enter speed down mode.

Power Button Function

This item is used to handle soft power on/off regardless of time counting (generally speaking, it is 4 sec) if you set it to *On/Off*. You can easily power on/off system by pressing the power button directly. This feature is only available on system with the ATX power control interface. If you use a standard AT power supply, this option will be ignored. In the "Suspend" setting, the system will be forced into suspend mode when turned off unless the power button is simultaneously pressed for more than 4 seconds to get in the Soft off function.

Ring Resume From Soft Off

This item will be used to wake up system from remote ringing control under Soft Off condition. If the "Disabled" setting is chosen, the system will not be resumed by modem ring.

PCI/Plug and Play Setup

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system which allows I/O devices to operate at speeds nearing CPU's when they communicate with their own special components. All of the options described in this section are important and technically complex. It is strongly recommended that only experienced users make any changes to the default settings.

Plug and Play Aware O/S

Set this option to "Yes" if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to "No" if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP.

NOTE

You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

Clear NVRAM

This option is used to clear NVRAM and check or update ESCD (Extended System Configuration Data) data after system power on. Setting this option to *No* will not clear NVRAM and the operation of update ESCD is effective in different ESCD data comparison. If you select the “Yes” setting, then the BIOS will update ESCD each time of power on.

PCI Latency Timer (PCI Clocks)

This option is used to control PCI latency timer period (follow PCI clocks). Based on PCI specification 2.1 or later and PCI bus frequency in the system, different timers can be selected to meet the PCI bus environment.

PCI VGA Palette Snoop

Some display cards that are non-standard VGA such as graphics accelerations or MPEG video cards may not show colors properly. User can choose “Enabled” setting to correct this display mismatch problem and support any ISA adapter card installed in the computer that requires VGA palette snooping.

Allocate IRQ to PCI VGA

This option will be used to allocate IRQ for PCI VGA card. In general, some of PCI VGA cards need IRQ support.

PCI IDE BusMaster

Set this option to *Enabled* to specify that the IDE controller on the PCI local bus has bus mastering capability.

Off Board PCI IDE Card

This option specifies if an off board PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the SBC (Single Board Computer) where the off board PCI IDE controller card is installed. If an off board PCI IDE controller is used, the onboard controller on the SBC is automatically disabled. If *Auto* is selected, BIOS automatically determines the correct setting for this option. If you want to respectively control off board PCI IDE Primary/Secondary IRQ resources, you should set this option among *Slot 1* to *Slot 4*. Otherwise, all of these sub-options will be hidden and unavailable.

Off Board PCI IDE Primary/Secondary IRQ

This option specifies the PCI interrupt used by the primary/ secondary IDE channel on the off board PCI IDE controller. The settings are *Disabled*, *INTA*, *INTB*, *INTC*, *INTD*, or *Hardwired* for installing off-board non-compliant PCI IDE card.

PCI Slot 1/2/3/4 IRQ Priority

These options specify the priority IRQ to be used for any PCI devices installed in PCI expansion slots 1 through 4. The settings are *Auto* (AMIBIOS automatically determines the priority IRQ), (IRQ) *3*, *4*, *5*, *7*, *9*, *10*, or *11*.

DMA Channel 0/1/3/5/6/7

These options specify if the named DMA channel is available for using on the ISA/EISA bus or PnP (Plug & Play).

IRQ 3/4/5/7/9/10/11/12/14/15.

These options specify the bus that the named interrupt request lines (IRQs) are using. These options allow specific IRQs to be used by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use the PCI/PnP Setup to remove the IRQ by assigning the option to the ISA/EISA setting. All IRQs used by on-board I/O are configured as PCI/PnP.

Peripheral Setup

This section describes I/O resources assignment for all the on-board peripheral devices.

On Board FDC

If the user wants to install a different add-on super I/O card to connect floppy drives, set this field to *Disabled*. Otherwise, set it to *Auto* to cause BIOS to automatically determine if the floppy controller should be enabled.

On Board Serial Port A/Port B

These fields control the resource assignments of two on-board serial interfaces, SIO1 and SIO2. The following lists show current options in On Board Serial

Port A/ Port B :

Auto	**c**annot set serial I/O resources by manual operation
Disabled	indicates on-board COM port function is ineffective
3F8h/COM1	assign I/O address 3F8h to COM1
2F8h/COM2	assign I/O address 2F8h to COM2
3E8h/COM3	assign I/O address 3E8h to COM3
2E8h/COM4	assign I/O address 2E8h to COM4

On Board IR Port

This option controls the resource assignments of on-board serial port 3. The IR Mode Select has three settings -- IrDA, ASK IR, and FIR.

On Board Parallel Port

There are four optional items, *Parallel Port Mode*, *EPP Version*, *Parallel Port IRQ*, and *Parallel Port DMA Channel,* used to control the on-board parallel port interface while the I/O base address is manually selected. The following list shows the available options of on-board parallel port:

Auto	user can not control all of LPT port I/O resources
Disabled	on-board parallel port function is ineffective and N/A
378h	locate IRQ7 for this default I/O address
278h	assign this I/O address to LPT1
3BCh	assign this I/O address to LPT1

Parallel Port Mode :

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options “Normal”, “Bi-Dir”, “EPP”, and “ECP”. The optimal default setting is *Bi-Dir*.

Setting	Description
Normal	Uni-directional operation at normal speed
Bi-Dir	Bi-directional operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.

EPP Version :

This option is only valid if the **Parallel Port Mode** option is set to *EPP*. It specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS.

Parallel Port IRQ :

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port.

Parallel Port DMA Channel :

This option is only available if **On Board Parallel Port** is set to fixed I/O address and the setting of **Parallel Port Mode** is ECP. This option sets the DMA channel used by ECP-capable parallel port.

On Board IDE

This option specifies the on board IDE controller channels that will be used. The settings are *Disabled*, *Primary*, *Secondary*, or *Both*.

Hardware Monitor Setup

This setup describes current system status detected by the hardware monitor controller. The status showed on screen will include :

l Current System and CPU Temperature

l Current CPU Fan Speed

l System operating voltage includes " Vcore", " Vtt", "Vio", "+5V", "+12V", "-12V", and "-5V".

BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the error and explaining the problem in detail so that it can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot a faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.27 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution:

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be started.
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack next.
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will be transferred to segment 0.
D6	Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum. If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution:

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the base 512KB memory test.
E1	Initializing the interrupt vector table next.
E2	Initializing the DMA and Interrupt controllers next.
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A:
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.
F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.
FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BAT command test.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End> or <Ins> keys were pressed during power on.
12	To initialize CMOS if the *initialize CMOS RAM in every boot* is set or the <End> key is pressed. Going to disable DMA and Interrupt controllers.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.

Uncompressed Initialization Codes (Continued)

Code	Description
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking is over. Setting the display mode next.
37	he display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.
3A	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.

Uncompressed Initialization Codes (Continued)

Code	Description
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory test.
48	Patterns written in base memory. Determining the amount of memory below 1MB next.
49	The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next.
4B	The amount of memory above 1MB has been found and verified. Checking for a soft reset and clearing the memory below 1MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next.
4D	The memory above 1MB has been cleared via soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64KB memory size next.
4F	Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next.
50	Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1MB next.
52	The memory above 1MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	he A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59	The *Hit <DEL>* message is cleared. The <*WAIT*…> message is displayed. Staring the DMA and interrupt controller test next.
60	The DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.

Uncompressed Initialization Codes (Continued)

Code	Description
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard Controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	Command byte written, Global data init done. To check for lock-key.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	The programming after Setup has completed. Displaying the power on Screen message next.
8B	The first screen message has been displayed. The <WAIT…> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.

Uncompressed Initialization Codes (Continued)

Code	Description
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot loader next.

Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact technical support to get this utility if necessary.

NOTE

Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, etc.) in the CONFIG.SYS files before running Flash programming utility.

Appendix 1 - Glossary of Terms

B

backplane: A device inside the chassis that contains slots, or sockets, for plugging in cards or cables.

bidirectional parallel port: An eight-bit port that can be used for an input as well as an output device.

bus: One or more electrical conductors that transmit power or binary data to the various sections of a computer or any common pathway between hardware devices. A computer bus connects the CPU to its main memory and the memory banks that reside on the control units of the peripheral devices. It is made up of two parts. Addresses are sent over the address bus to signal a memory location, and the data are transferred over the data bus to that location.

C

card cage: A cabinet or metal frame that holds printed circuit cards.

CMOS (Complementary Metal Oxide Semiconductor): A technique of arranging transistors which uses very low power.

D

disk access LED: The LED located on the front control panel that indicates when the hard disk drive is active.

DRAM (Dynamic Random Access Memory): The main memory in your computer. It needs to be refreshed by a memory controller or it loses its information.

drive bay: Area in the chassis where drives are mounted.

E

electrostatic discharge (ESD): Stationary electrical charges in which no current flows. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.

Appendix 1 - Glossary of Terms

EMI (ElectroMagnetic Interference): Noise generated by the switching action of the power supply and other system components. Conducted EMI is interference generally conducted into the power line, and is normally controlled with a line filter. Radiated EMI is that portion that radiates into free space. One way to suppress it is by enclosing circuitry in a metal case.

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power.

expansion card: A printed circuit board that plugs into an expansion slot.

F

floppy drive: A device for reading the information contained on external, portable computer disks called floppy disks.

front control panel: The small panel on the front of the computer that contains the power switch, reset switch, Power ON LED, the disk access LED, and the keyboard connector.

H

hard drive: A data storage device. Hard drives magnetically store computer data on spinning internal disks.

hold-down bar: A metal bar located in the I/O bay of the chassis. It is used to keep I/O cards firmly seated in their slots. (There is no hold-down bar in CompactPCI systems.)

I

IDE (Integrated Drive Electronics): A standard of signalling and communicating with a device.

I/O card: A printed circuit board that plugs into an I/O slot.

I/O slot: A slot for plugging in additional I/O cards to expand the capability of a computer.

ISA: The original IBM/PC clone plug-in board standard.

K

keyboard connector: The five-pin connector located on the front control panel.

kilobyte (KB): 1,024 bytes.

L

LED: Light Emitting Diode. Long-lasting light emitters usually used as indicators.

load board: A board having specific resistance to current flow.

P

parallel port: I/O connector used to hook up a printer or other parallel interface device. The parallel port is usually a 25-pin female DB25 connector.

PCI(Peripheral Component Interconnect): An optional slot standard for plug-in boards

port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

power good: Signal used to prevent the computer from starting until the power has stabilized. The power good line switches from 0 to +5 volts within one tenth to one half second after the power supply reaches normal voltage levels. Whenever low input voltage causes the output voltage to fall below operating levels, the power good signal goes back to zero.

power ON/diagnostic LED: The LED located on the front control panel that indicates that power is present in the computer.

power supply: Electrical system that converts AC current from the wall outlet into the DC currents required by the computer circuitry. In a personal computer, +5, -5, +12 and -12 voltages are generated.

power switch: Located on the front control panel, the power switch turns power ON to the computer.

R

RAID (Redundant Array of Independent Disks): A storage technology using an array of two or more disks to redundantly store information. If one disk fails in a RAID array, the unit continues to function without loss of data.

RAM (Random Access Memory): The memory used to execute applications while your computer is turned ON. When you turn your computer OFF, all data stored in RAM is lost.

real-time clock (RTC): A periodic interrupt used to derive local time.

reset switch: Button or key that reboots the computer. All current activities are stopped cold and any data in memory are lost.

retaining bracket: The bracket on the back of the chassis that holds connectors from the board, usually a DB9 for serial port, a DB25 for parallel port, and mini-DIN connectors for keyboard and mouse.

S

SCSI (Small Computer System Interface): A high speed, general purpose interface to storage devices.

serial port: A two-channel port, one channel used for ”In” transmissions and one for ”Out” transmissions.

W

watchdog timer: A device that watches for CPU inactivity and then resets the CPU after a specified duration of inactivity.

LIMITED WARRANTY

I-Bus/Phoenix warrants this product to be free of defects in material and workmanship for an initial period of two (2) years from date of delivery to the original purchaser from I-Bus/Phoenix.

During this period, I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, except as set forth in this warranty agreement.

I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, if the defect is related to the I-Bus/Phoenix manufactured product, such as power supply, backplanes, other chassis components, or CPUs. I-Bus/Phoenix is not liable for any defects in material or workmanship of any peripherals, products or parts which I-Bus/Phoenix does not design or manufacture. However, I-Bus/Phoenix will honor the original manufacturer's warranty for these products.

I-Bus/Phoenix will analyze the defective component and the customer will be charged in the following instances:

- No problem found: $75 (U.S. dollars).
- Damage: parts and labor at $75 per hour with a $100 minimum charge (U.S. dollars). Receipt of damaged goods voids the I-Bus/Phoenix warranty.

Repair parts and replacement products will be furnished on an exchange basis and will be either new or reconditioned. All replacement parts and products shall become the property of I-Bus/Phoenix, if such parts or products are provided under this warranty agreement. In the event a defect is not related to the I-Bus/Phoenix manufactured product, I-Bus/Phoenix shall repair or replace the defective parts at purchaser's cost and deliver the defective parts to the purchaser.

This Limited Warranty shall not apply if the product has been misused, carelessly handled, defaced, modified or altered, or if unauthorized repairs have been attempted by others.

The above warranty is the only warranty authorized by I-Bus/Phoenix and is in lieu of any implied warranties, including implied warranty of merchantability and fitness for a particular purpose.

In no event will I-Bus/Phoenix be liable for any such damage as lost business, lost profits, lost savings, downtime or delay, labor, repair or material cost, injury to person or property or any similar or dissimilar consequential loss or damage incurred by purchaser, even if I-Bus/Phoenix has been advised of the possibility of such losses or damages.

In order to obtain warranty service, the product must be delivered to the I-Bus/Phoenix facility, or to an authorized I-Bus/Phoenix service representative, with all included parts and accessories as originally shipped, along with proof of purchase and a Returned Merchandise Authorization (RMA) number.

The RMA number is obtained, in advance, from I-Bus/Phoenix Customer Service Department and is valid for 30 days. The RMA number must be clearly marked on the exterior of the original shipping container or equivalent. Purchaser will be responsible and liable for any missing or damaged parts. Purchaser agrees to pay shipping charges one way, and to either insure the product or assume the liability for loss or damage during transit. Ship to:

I-Bus/Phoenix

ATTENTION: RMA REPAIR DEPT.

RMA ####

8888 Balboa Avenue

San Diego, CA 92123

Appendix 2 - Limited Warranty

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Appendix 3 - FCC Information

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

WARNING: This equipment has been tested and found to comply with the limits for a Class "A" digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This product was FCC verified under test conditions that included the use of shielded I/O cables and connectors between system components. To be in compliance with FCC regulations, the user must use shielded cables and connectors and install them properly.

Appendix 3 - FCC Information

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