IBC2901

Celeron® / Dual Pentium III®
ISA/PCI Single Board Computer
with Video and Dual Ethernet

User's Guide

Doc No. Part No. 100851 Rev B

Customer Service

Worldwide Headquarters
I-Bus Corporation
3350 Scott Blvd, Building 54
Santa Clara, CA 95054
USA
Phone : +1 (408) 450-7880
Fax : +1 (408) 450-7881
Toll Free: 877-777-IBUS
Email: contact.us@ibus.com

European Headquarters
I-Bus
Unit 6, Chichester Business Park
City Fields Way, Tangmere
West Sussex, PO20 2LB, UK
Tel: +44 (0) 1243 756300
Fax: +44 (0) 1243 756301
Email: contact.uk@ibus.com

France, Italy
I-Bus
B.P 45 Valbonne
06901 Sophia Antipolis CEDEX
France
Tel: +33 (0) 493 004 360
Fax: +33 (0) 493 004 369
Email: contatct.fr@ibus.com

Other countries, please contact support@ibus.com

Thank You
from the

team for
purchasing this product

I-Bus
Computing Systems

Dear Customer,

Thank you for purchasing an I-Bus product. We hope that this product exceeds your expectations. It is our desire to provide you with accurate, up-to-date information about the product(s) you have purchased. We welcome your comments and suggestions about our manuals.

You may email those comments and suggestions to support@ibus.com. Please be sure to include your name, the name of your company, the product you purchased, and the document number/revision (i.e. 0000000 Rev. *). This number is located on the title page.

At I-Bus, we value our customers and partners, and you can continue to count on I-Bus/Phoenix to be customer focused and to provide you a large range of solutions -- from cost-effective to fully customized industrial computer solutions.

Again, thank you for your commitment to I-Bus. We appreciate your business and look forward to continuing to work with you and helping you reach your goals.

I-BUS

Infini-Availability™

Chapter 1. Introduction

Chapter 2. Configuration and Installation

This page was intentionally left blank

1. Introduction

1.1. Important Safety Instructions

1.2. LITHIUM BATTERY REPLACEMENT

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

1.3. Product Description

The IBC2901 is a PCI/ISA single board computer designed to support a wide range of processing options. Processor options range from a single Intel® Celeron™ to a dual Pentium III®. The IBC2901 supports up to 768Mbytes of Synchronous DRAM and up to 64Mbytes of ATA Flash Drive. Additional features include dual 10/100 Base-TX Ethernet channels, PMC expansion, and built-in AGP SVGA video. The IBC2901 also supports a full set of standard PC peripherals: IDE, floppy, USB, serial, parallel, mouse, and keyboard. Additional industrial features include serial port console redirection, battery-backed real time clock, CPU temperature monitors, and a watchdog timer.

The IBC2901 I/O panel connectors include VGA, dual Ethernet, USB and combination Mouse/Keyboard. The IBC2901 supports a PMC mezzanine board for applications that require additional PCI functions.

1.4. Standard Features

- Full size SBC with PCI/ISA connectors
- Supports Single or Dual Pentium® III Processors up to 850MHz
- Supports Single Celeron™ processors up to 533MHz
- 256Kbytes Integrated L2 Cache on Pentium® III Processors

- 128Kbytes Integrated L2 Cache on Celeron™ Processors
- Up to 768Mbtyes of SDRAM
- Up to 64Mbytes of ATA Flash disk
- Dual 10/100 Base-TX Ethernet Channels (I/O panel)
- AGP SVGA Video Support up to 1600x1200x64K (I/O panel)
- Flat Panel Support for TFT/STN Panels
- PCI Mezzanine Card (PMC) Expansion
- 512 Kbytes of Flash for System BIOS
- Battery-Backed CMOS and Real Time Clock
- Watchdog Timer
- Supply Voltage, Temperature and Fan Speed Sensors
- Standard PC Peripherals:
    - Ultra IDE
    - Floppy
    - USB (I/O panel)
    - Two Serial Ports
    - One Parallel Port
    - Mouse/Keyboard (I/O panel)
- Microsoft Windows® Compatible

Functional Blocks

A functional block diagram for the IBC2901 is shown in Figure 1-1. The major functional blocks are discussed in detail below.

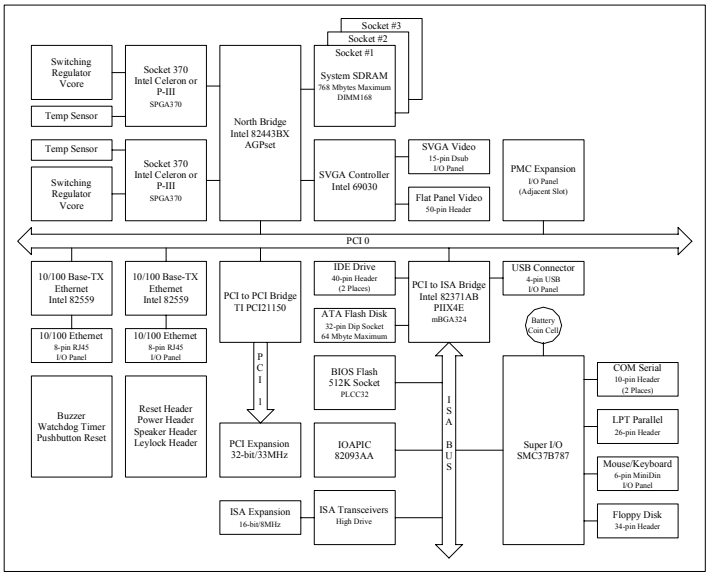


Figure 1-1. IBC2901 Functional Block Diagram

1.4.1. Processor Architecture

The IBC2901 CPU architecture includes two PGA370 sockets. This architecture supports a wide range of options from a single Intel Celeron processor up to dual Pentium III processors. These processors feature an internal temperature transducer to permit the application software to monitor the CPU temperature. A 3-pin header is located near each processor socket to power a +12V fan. The fan speed may also be monitored by the application software.

1.4.2. System DRAM

The IBC2901 includes three 168-pin DIMM sockets. Each of these sockets support 3.3V PC100 synchronous DRAM modules currently available in densities up to 256 Mbytes. Fully populated, this adds up to 768 Mbytes of system DRAM.

1.4.3. BIOS Flash

The system BIOS is contained in a single 512Kbyte Flash loaded into a 32-pin PLCC socket. The Flash write strobe signal includes a series zero-ohm resistor that can be removed to permanently disable the write operation.

1.4.4. IDE and ATA Flash Disk

The IBC2901 supports a primary and secondary IDE channel. The primary IDE channel is connected to both a 40-pin header and to the ATA Flash Disk socket. Jumpers are available to select which device is the master and which is the slave. The secondary IDE channel is connected to separate 40-pin header.

The ATA Flash Disk socket is 32-pin DIP socket that accepts an ATA-compatible Flash disk in sizes up to 64Mbytes.

1.4.5. PMC Expansion

The PCI Mezzanine Card (PMC) standard defines the connector pin assignments and mechanical dimensions for a mezzanine board based on a PCI interface. The PMC architecture is compliant with IEEE® 1386 for a 32-bit implementation. An optional PMC carrier board elevates the PMC card to line up with the adjacent slot assuming a 0.8-inch spacing. This is illustrated in Figure 1-2.

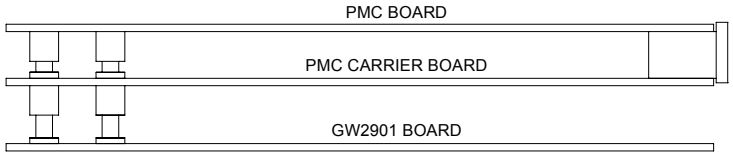


Figure 1-2. PMC Carrier Board Mounting

1.4.6. AGP Video

The IBC2901 includes an Intel 69030 Advanced Graphics Port (AGP) SVGA controller with 4Mbytes of video memory. The video controller supports dual independent display output pipelines to drive two different displays with either the same image or different images. The video controller supports display resolutions up to

1600X1200X64K color in single display mode and display resolutions up to 1280X1024X256 color in dual display mode.

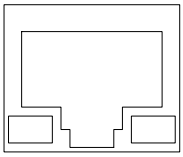
In addition to standard VGA monitors, the video controller supports a wide range of flat panels. This includes TFT, DSTN, SSTN, EL, and Plasma.

The SVGA is available through an industry standard 15-pin D-shell connector located on the I/O panel. The flat panel is available through a 50-pin header in a 2 row by 25 pin configuration with a 0.050-inch spacing.

1.4.7. Ethernet

The Ethernet interfaces are based on an Intel 82559ER 10/100 Base-TX Ethernet controller. The Intel 82559ER is a 32-bit PCI device that includes both the Media Access Controller (MAC) and the Physical Layer Controller (PHY). The MAC supports 10 Mbps and 100 Mbps operation compliant with the IEEE 802.3 standard. The PHY supports 10 Base-T and 100 Base-TX compliant with the IEEE 802.3 standard.

The Ethernet ports are available at the I/O panel through industry standard 8-pin RJ45 connectors. Each connector includes two light emitting diodes (LEDs). The green LED indicates LINK/ACTIVITY and the yellow LED indicates LINK SPEED. The LINK/ACTIVITY LED in on when a link is established and blinks when there is activity. The LINK SPEED LED is off for 10Mbit operation and lights for 100Mbit operation.



GREEN (LINK/ACTIVITY) YELLOW (LINK SPEED)

Figure 1-3. Ethernet Status LEDs

1.4.8. PCI/ISA Interface

The IBC2901 is electrically and mechanically compatible with the PICMG 1.0 R2.0 specification. The 32-bit PCI interface includes a transparent bridge to ensure PCI signal integrity in a backplane architecture. The 16-bit ISA interface includes high-drive low-noise buffers to increase the drive capability to 20 slots.

1.4.9. Super I/O

The SMC FDC37B788 Super I/O includes a real time clock, keyboard/mouse controller, floppy disk interface, printer port and two serial ports. The serial ports interface through standard RS-232 signal levels at baud rates up to 115 Kbaud. A coin cell battery in a socket provides battery-backup for the real time clock. The minimum battery life is 5 years.

The keyboard and mouse interface are combined into a single 6-pin MiniDIN connector as is standard on many computers. This architecture requires a splitter cable to split the mouse and the keyboard interface into separate connectors. The floppy interface is available through a standard 34-pin header. The printer port interface is available through a standard 26-pin header. The serial ports are each available through standard 10-pin headers.

1.4.10. Hardware Monitor

A National Semiconductor LM87 Hardware Monitor provides CPU temperature, supply voltage, and fan speed monitoring.

1.4.11. Watchdog Timer

A watchdog timer optionally monitors system operation to be sure that application software is executing as designed. The watchdog timer generates hardware reset if the application software fails to strobe the watchdog timer with a minimum time interval. Watchdog timer operation is discussed in more detail in the next chapter.

1.4.12. DC/DC Converter

The IBC2901 includes dual DC/DC converters for supplying each processor with its own core voltage. These converters are based upon the Linear Technology LTC1709 2-phase synchronous step-

down current mode switching controller and have been designed to meet the Intel VRM8.4 specification. These converters can supply core voltages ranging from 1.3 to 2.05V.

This page was intentionally left blank

2. Configuration and Installation

2.1. Memory and I/O Mapping

There are several memory and I/O devices local to the IBC2901. There are also expansion sites for adding memory and I/O resources. The address maps for these devices are shown below.

Memory Space	Memory Address (hex)	Description
768M - 4G	30000000 – FFFFFFFF	Available
1M - 768M	00100000 – 2FFFFFFF	***System Memory***
896K - 1024K	000E0000 – 000FFFFF	System BIOS
800K - 896K	000C8000 – 000DFFFF	BIOS Expansion
768K - 800K	000C0000 – 000C7FFF	VGA BIOS
640K - 768K	000A0000 – 000BFFFF	VGA DRAM
0K - 640K	00000000 – 0009FFFF	System DRAM

Table 2-1: Memory Map

I/O Address (hex)	Device
1035	General Purpose Outputs
1031	General Purpose Inputs
0CF8 – 0CFF	PCI Configuration
04D0 – 04D1	Interrupt Controller
0480 – 048F	DMA Page
03F8 – 03FF	COM1
03F6 – 03F7	Primary IDE
03F0 – 03F7	Floppy & IDE
0376 – 0377	Secondary IDE
0370 – 0371	Super I/O
02F8 – 02FF	COM2
01F0 – 01F7	Primary IDE
0170 – 0177	Secondary IDE
00F0 – 00F1	Coprocessor
00C0 – 00DF	DMA Controller
00A0 – 00A1	Interrupt Controller
0092	Port 92 Control
0081 – 008F	DMA Page
0070 – 0071	Real Time Clock
0060 – 0064	Keyboard Controller
0040 – 0043	Timer/Counters
0020 – 0021	Interrupt Controller
0000 – 000F	DMA Controller

Table 2-2: I/O Map

2.2. PCI Device Mapping

The IBC2901 includes the PCI device mapping listed below.

Bus Number	Device Number	**Fcn Number**	**Vendor ID**	**Device ID**	**Description**
00	00	00	8086	7190	Intel 82443BX North Bridge
00	01	00	8086	7191	Intel 82443BX AGP Bridge
00	07	00	8086	7110	Intel 82371EB South Bridge (PIIX4E)
00	07	01	8086	7111	Intel 82371EB IDE
00	07	02	8086	7112	Intel 82371EB USB
00	07	03	8086	7113	Intel 82371EB ACPI
00	0C	00	8086	1209	Ethernet
00	0D	00	8086	1209	Ethernet
00	0F	00	104C	AC28	PCI to PCI Bridge
01	09	00	1026	0C30	AGP Video

Table 2-3: PCI Device Map

2.3. Interrupt Mapping

The IBC2901 includes the standard PC-compatible interrupt architecture for monitoring 15 interrupt inputs. The interrupt sources are shown in the following table. PCI interrupts are level sensitive and are shared between on-board PCI devices and CompactPCI peripherals.

Interrupt	**Function**
0	System Timer
1	Keyboard
2	Slave Interrupt Controller
3	COM2 Serial
4	COM1 Serial
5	PCI
6	Floppy
7	LPT Parallel
8	Real Time Clock
9	PCI
10	PCI
11	PCI
12	Mouse
13	Coprocessor
14	IDE Primary
15	IDE Secondary

Table 2-4: Interrupt Sources

2.4. Parallel I/O

The IBC2901 includes parallel I/O bits accessible through the 82371EB PIIX4E South Bridge for controlling and monitoring various functions. These bits are accessed at I/O location 1031h for input functions and 1035h for output functions. The operation for each of these bits is listed in the following table. See the Intel 82371EB data sheet for more information on programming these registers. Please note that care should be taken not to program RESERVED bits.

Port	Bit	Description
1031h (Inputs)	0 1-2 3 4-7	LM87 THERM# Status Signal Reserved LM87 ALERT# Status Signal Reserved
1035h (Outputs)	0 1 2 3 4-7	Reserved CPU Fan Control (J14) - 0 = OFF, 1 = ON * CPU Fan Control (J15) - 0 = OFF, 1 = ON * Watchdog Enable - 1 = ON (Armed), 0 = OFF * Reserved

*Default value after reset

Table 2-5: Board Specific I/O

2.5. Watchdog Control

A Dallas Semiconductor DS1819A reset monitor is used on the IBC2901 to provide a watchdog timer. The watchdog strobe input is driven with a constant clock source. The clock source is gated with an enable bit. When the enable bit is low (x1035h bit 3 is written to 0) the clock strobes the watchdog. When this bit is high the clock shuts off and the watchdog timer is activated. Once activated, the enable bit must be driven low within 1.12 seconds to reset the timer. A sample routine for controlling the watchdog timer is shown below.

ACTIVATE WATCHDOG

```
IN      AL,1035h
OR      AL,08h
OUT     1035h,AL
```

STROBE WATCHDOG

```
IN      AL,1035h
AND     AL,F7h
OUT     1035h,AL
OR      AL,08h
OUT     1035h,AL
```

2.6. Push Button Reset

A push button reset switch is provided on the IBC2901 for use during application development. The switch is labeled S1 and is located along the bottom edge of the board to the left of the PCI edge finger connector.

2.7. Serial Console Redirection

The IBC2901 supports console redirection through the COM1 serial port. The BIOS will go out during initialization and check to see if the RIN and DTR pins of the COM1 serial port are tied together and if so will redirect the console to the serial port. A standard ASCII terminal program such as HyperTerminal may then be used to communicate with the IBC2901. Only text output is supported when using console redirection.

The serial connector is configured as DTE. A null modem adapter or cross over cable is required to communicate with another DTE device.

The terminal program should be set to 9600 Baud, 8 data bits, no parity, 1 stop bit (8N1). Flow control should be set for no hardware or software handshaking and the terminal should be set for standard ANSI emulation.

2.8. Clearing CMOS

Setup information for the IBC2901 is contained in battery backed memory inside of the Super I/O controller. To clear this information and reset the board to the BIOS defaults follow the below steps:

1. Turn off system power.
2. Move jumper W1 from position 1-2 to position 2-3 and then back.

The battery supplied with the IBC2901 is a standard CR2032 coin cell rated for 210mAH. The battery life is approximately 70K hours (8 years).

2.9. BIOS Update

The BIOS for the IBC2901 is located in a 512 Kbyte Flash memory located in the 32-pin PLCC socket (U22). It can be updated using the I-Bus/Phoenix FLASH.EXE utility. Contact I-Bus/Phoenix for the latest BIOS and Flash utility.

Follow the below steps to update the BIOS.

1. Power the IBC2901 and boot to a DOS prompt.
2. Type FLASH.EXE gw2901.BIN
3. Power cycle the computer.

2.10. ATA Flash Drive Configuration

The IBC2901 contains a 32-pin socket designed to accept an optional ATA Flash Drive. The socket is designated as connector J17. The ATA Flash Drive shares the primary IDE interface with the 40-pin header designated as connector J9. The ATA Flash Drive and the 40-pin header are configured for master and slave operation using jumpers W2 and W4. Installing jumper W2 configures the ATA Flash Drive as a master. Installing W4 configures the 40-pin header as a master. DO NOT install W2 and W4 at the same time. Jumper W3 is used to write-protect the ATA Flash Drive. Installing jumper W3 enables write-protection to inhibit any further data storage to the ATA Flash Drive.

2.11. Flat Panel Interface

An optional flat panel interface connector is provided for interfacing to standard TFT/STN panels. The flat panel connector is designated as J24. For information on interfacing to different flat panels see the Asiliant (formerly Chips and Technologies) 69030 datasheet. See the flat panel connector specification section in this chapter for pin assignments.

2.12. Hardware Monitor

Supply voltage, CPU temperature and fan speed can be monitored with the on-board National Semiconductor LM87 hardware monitor. The LM87 uses the 82371EB (PIIX4E) South Bridge SMBus controller for communication. The LM87's SMBus address is 0101100. See the LM87 and PIIX4E datasheets for more information on programming.

The IBC2901 Drivers and Utilities disk contains a monitor program called GWMON.EXE for displaying CPU temperatures, fan speeds and voltages. This application runs under Windows 95/98/NT.

2.13. Interface Connectors

The IBC2901 connector pin assignments and signal descriptions are included in the following sections.

- J1: DRAM Socket 2
- J2: DRAM Socket 3
- J3: Speaker
- J4: IDE Secondary
- J5: COM2 Serial
- J6: LPT Parallel
- J7: DRAM Socket 1
- J8: Coin Cell Battery
- J9: IDE Primary
- J10: IDE Activity LED
- J11: Reserved
- J12: IrDA
- J13: COM1 Serial
- J14: Floppy
- J15: CPU 1 Fan
- J16: CPU 2 Fan
- J17: ATA Flash Drive
- J18: SVGA Video
- J19: CPU 1
- J20: CPU 2
- J21: Mouse & Keyboard
- J22: Ethernet 1
- J23: Reset
- J24: Flat Panel Video
- J25: PMC Expansion
- J26: PMC Expansion
- J27: Ethernet 2
- J28: USB
- J29: Auxiliary Power

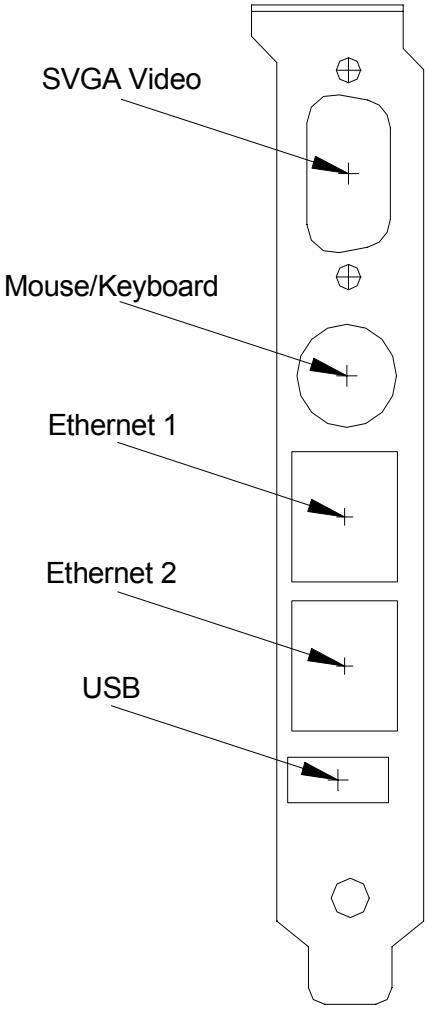


Figure 2-1. I/O Panel

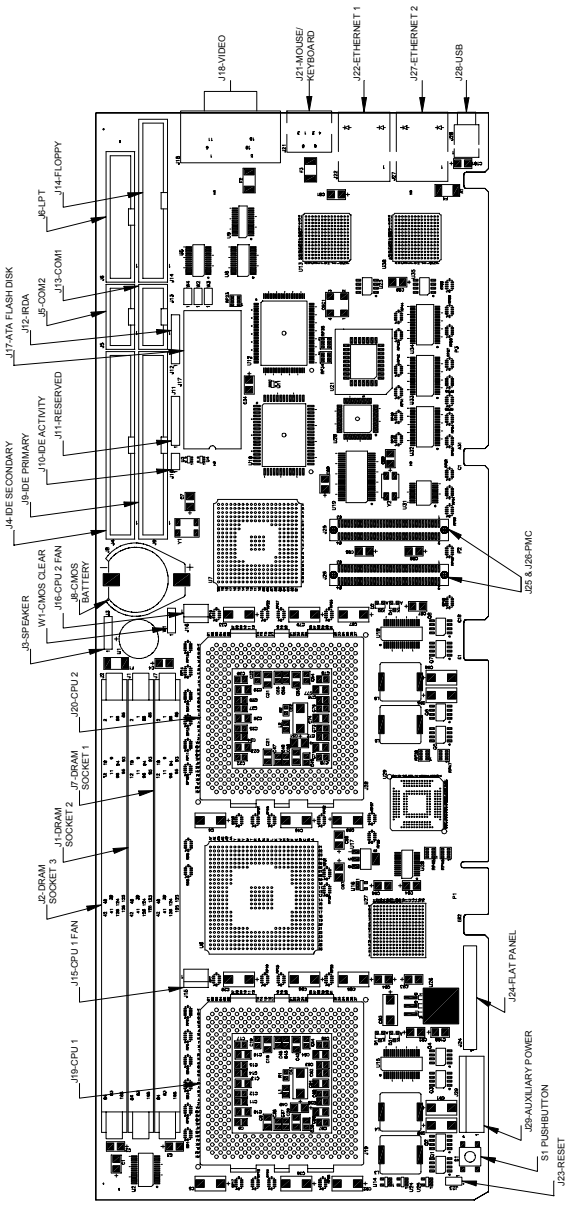


Figure 2-2. Connector Locations

2.13.1. DIMM Sockets (J1, J2 and J7)

These sockets accept industry standard 168-pin DIMM memory modules. The modules must be 3.3V, PC100, SDRAM. Maximum supported DIMM size is 256MB allowing for a maximum of 768Mbytes.

2.13.2. Speaker Connector (J3)

Pin Number	Signal
1	Fused 5V
2	GND
3	GND
4	SPEAKER

Table 2-6: Speaker Pin Assignment

2.13.3. Primary (J9) and Secondary (J4) IDE Connectors

Pin	Signal	Pin	Signal
1	RESET#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	DREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	Pull Up
29	DACK#	30	GND
31	INTRQ	32	No Connect
33	ADR1	34	DIAG#
35	ADR0	36	ADR2
37	CS1#	38	CS1#
39	DASP#	40	GND

Table 2-7: Primary and Secondary Pin Assignment

2.13.4. COM1 (J13) and COM2 (J5) Connectors

Pin	Signal	Pin	Signal
1	DCD#	2	DSR#
3	RXD	4	RTS#
5	TXD	6	CTS#
7	DTR#	8	RIN#
9	GND	10	No Connect

Table 2-8: COM1 and COM2 Pin Assignment

2.13.5. LPT Parallel Connector (J6)

Pin	Signal	Pin	Signal
1	STB#	2	AFD#
3	D0	4	ERR#
5	D1	6	INIT#
7	D2	8	SLIN#
9	D3	10	GND
11	D4	12	GND
13	D5	14	GND
15	D6	16	GND
17	D7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PEND	24	GND
25	SLCT	26	No Connect

Table 2-9: LPT Pin Assignment

2.13.6. Coin Cell Battery (J8)

The coin cell battery holder is designed to accept a standard 3V coin cell battery with a CR2032 footprint. The holder is polarized so that the positive terminal of the battery should be visible when the battery is installed. The positive battery terminal is generally marked with a "+".

2.13.7. IDE Activity LED Connector (J10)

Pin Number	Signal
1	Current Limited 5V
2	ACTIVITY

Table 2-10: IDE Activity LED Pin Assignment

2.13.8. IrDA Connector (J12)

Pin Number	Signal
1	RXD
2	TXD
3	GND
4	5V
5	No Connect
6	5V

Table 2-11: IrDA Pin Assignment

2.13.9. Floppy Connector (J14)

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	GND	4	No Connect
5	No Connect	6	DRATE0
7	GND	8	INDEX#
9	GND	10	MOTR1#
11	GND	12	DRIVE2#
13	GND	14	DRIVE1#
15	GND	16	MOTR2#
17	GND	18	DIR#
19	GND	20	STEP#
21	GND	22	WDATA#
23	GND	24	WGATE#
25	GND	26	TRAK0#
27	GND	28	WPRT#
29	GND	30	RDATA#
31	GND	32	HDSEL#
33	GND	34	DSKCHG#

Table 2-12: Floppy Pin Assignment

2.13.10. CPU 1 Fan (J15) and CPU 2 Fan (J16) Connectors

Pin Number	Signal
1	Fan Control
2	12V
3	Fan Tachometer

Table 2-13: CPU Fan Pin Assignment

2.13.11. ATA Flash Drive Socket (J17)

Pin	Signal	Pin	Signal
1	RESET#	32	5V
2	D7	31	D8
3	D6	30	D9
4	D5	29	D10
5	D4	28	D11
6	D3	27	D12
7	D2	26	D13
8	D1	25	D14
9	D0	24	D15
10	WP#	23	IOW#
11	IOR#	22	CSEL
12	INTRQ	21	No Connect
13	ADR3	20	PDIAG#
14	ADR1	19	ADR2
15	CS1#	18	CS3#
16	GND	17	DASP#

Table 2-14: ATA Flash Drive Pin Assignment

2.13.12. SVGA Video Connector (J18)

Pin Number	Signal
1	RED
2	GREEN
3	BLUE
4	No Connect
5	GND
6	GND
7	GND
8	GND
9	Fused 5V
10	GND
11	No Connect
12	SDAT
13	HSYNC
14	VSYNC
15	SCLK

Table 2-15: SVGA Video Pin Assignment

2.13.13. CPU 1 and CPU 2 Sockets (J19 and J20)

The sockets used to accept either a single or a dual CPU.

2.13.14. Mouse and Keyboard Connector (J21)

Pin Number	Signal
1	Keyboard Data
2	Mouse Data
3	GND
4	Fused 5V
5	Keyboard Clock
6	Mouse Clock

Table 2-16: Mouse and Keyboard Pin Assignment

2.13.15. Ethernet 1 (J22) and Ethernet 2 (J27) Connectors

Pin Number	Signal
1	TX+
2	TX-
3	RX+
4	Termination
5	Termination
6	RX-
7	Termination
8	Termination

Table 2-17: Ethernet Pin Assignment

2.13.16. Reset Connector (J23)

Pin Number	Signal
1	RESET#
2	GND

Table 2-18: Reset Pin Assignment

2.13.17. Flat Panel Video Connector (J24)

Pin	Signal	Pin	Signal
1	5V	2	GND
3	GND	4	SHFCLK
5	5V	6	GND
7	GND	8	LP
9	FLM	10	GND
11	PD0	12	PD1
13	PD2	14	PD3
15	GND	16	PD4
17	PD5	18	PD6
19	PD7	20	GND
21	PD8	22	PD9
23	PD10	24	PD11
25	GND	26	PD12
27	PD13	28	PD14
29	PD15	30	GND
31	PD16	32	PD17
33	PD18	34	PD19
35	GND	36	PD20
37	PD21	38	PD22
39	PD23	40	GND
41	M	42	ENBKL
43	ENVDD	44	ENVEE
45	12V	46	GND
47	12V	48	GND
49	No Connect	50	No Connect

Table 2-19: Flat Panel Pin Assignment

2.13.18. PMC Connector (J25)

Pin	Signal	Pin	Signal
1	No Connect	2	No Connect
3	GND	4	INTA#
5	INTB#	6	INTC#
7	No Connect	8	5V
9	INTD#	10	No Connect
11	GND	12	No Connect
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	5V
19	5V	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	CBE3#
27	AD22	28	AD21
29	AD19	30	5V
31	5V	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	5V
39	GND	40	LOCK#
41	No Connect	42	No Connect
43	PAR	44	GND
45	5V	46	AD15
47	AD12	48	AD11
49	AD09	50	5V
51	GND	52	CBE0#
53	AD06	54	AD05
55	AD04	56	GND
57	5V	58	AD03
59	AD02	60	AD01
61	AD00	62	5V
63	GND	64	Pull Up

Table 2-20: PMC Pin Assignments

2.13.19. PMC Connector (J26)

Pin	Signal	Pin	Signal
1	12V	2	No Connect
3	No Connect	4	No Connect
5	No Connect	6	GND
7	GND	8	No Connect
9	No Connect	10	No Connect
11	5V	12	3.3V
13	RESET#	14	GND
15	3.3V	16	GND
17	No Connect	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V
25	AD22 (IDSEL)	26	AD23
27	3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	CBE2#
33	GND	34	No Connect
35	TRDY#	36	3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	3.3V	42	SERR#
43	CBE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD08	50	3.3V
51	AD07	52	No Connect
53	3.3V	54	No Connect
55	No Connect	56	GND
57	No Connect	58	No Connect
59	GND	60	No Connect
61	Pull Up	62	3.3V
63	GND	64	No Connect

Table 2-21: PMC Pin Assignments

2.13.20. USB Connector (J28)

Pin Number	Signal
1	Fused 5V
2	D-
3	D+
4	GND

Table 2-22: USB Pin Assignment

2.13.21. Auxiliary Power Connector (J29)

Pin Number	Signal
1	5V
2	5V
3	3.3V
4	GND
5	GND
6	GND

Table 2-23: Auxiliary Power Pin Assignment

2.14. Thermal Considerations

The IBC2901 operating temperature is limited by the CPU. The maximum operating temperature is dependant on the processors maximum case temperature (Tc) and the amount of cooling provided by the enclosure and fansink. The IBC2901 ships from the factory with a fansink for cooling the processor. The fansink has a thermal resistance of 1.2_C/W, thus for every Watt of power dissipation by the processor; the case temperature will rise by 1.2_C above ambient.

The chart below shows the maximum operating temperature for the processors currently shipping with the IBC2901. The operating temperatures are based upon a static environment with no forced air besides that provided by the processor's fansink and based upon Intel's maximum power dissipation numbers. To obtain higher operating temperatures, provide forced air-cooling. It is recommended that a complete thermal analysis be performed on the users enclosure to take into account the system's thermal properties. As different processors and fansinks become available, these numbers may change. Please contact the factory for the latest configurations.

CPU Model	CPU Case Temperature (Tc)	Max Design Power (W)	Operating Temperature
Celeron 366 MHz	0 – 85°C	21.7	0 – 59°C
PIII 750 MHz	0 – 80°C	24.5	0 – 50°C

Table 2-24: IBC2901 Operating Temperature

The fansink used on the IBC2901 is a double ball bearing design, which maximizes the mean time between failure (MTBF). The fan's MTBF is 24.7 years at 50°C and 12.3 years at 60°C.

2.15. Jumper Summary

The following table summarizes the function of the IBC2901's jumpers.

Jumper	Description
W1	CMOS Erase 1-2 = Battery enabled 2-3 = Battery disabled
W2	ATA Flash Drive Master/Slave Selection Installed = Master Removed = Slave
W3	ATA Flash Drive Write Protect Installed = Write Disabled Removed = Write Enabled
W4	40-pin IDE Header (J9) Master/slave Selection Installed = Master Removed = Slave

Table 2-25: IBC2901 Jumper Summary

2.16. Manufacturers' Website Links

The section provides links to manufacturers websites for parts and specifications used on the IBC2901.

PCI/ISA Specification

http://www.picmg.org

Chipset - Intel 440BX (82443BX, 82371EB PIIX4E)

http://developer.intel.com

Ethernet Controller - Intel 82559ER

http://developer.intel.com

AGP Video - Asiliant 69030

http://www.asiliant.com

Super I/O - Standard Microsystems FDC37B787

http://www.smsc.com

Hardware Monitor - National Semiconductor LM87

http://www.national.com

Watchdog - Dallas Semiconductor DS1819A

http://www.dalsemi.com

PCI to PCI Bridge - Texas Instruments PCI2050

http://www.ti.com

This page was intentionally left blank

3. BIOS Setup Options

3.1. Entering Setup Screen

The BIOS allows the user to configure the IBC2901 for various hardware and disk drive configurations. To enter the BIOS setup screen push the keyboard DELETE key during initial power-on. A blue screen will appear with several menu items. Use the up and down keyboard keys to select a particular menu item. Hit the ENTER key to enter into the sub-menu for that item.

To change the settings when in a sub-menu use the up and down arrow keys to select the sub-menu item and the “+” and “-“ keys to toggle between the options for that item.

Most of the items in the BIOS setup are pre-configured from the factory and should not need to be modified. The following sub sections give details for some of the more frequently used options.

3.2. Hard Disk Setup

The IBC2901 contains primary and secondary IDE channels thus allowing support of up to four IDE drives (primary master, primary slave, secondary master, secondary slave).

The setup screen for the IDE channels is in the Basic CMOS Configuration menu. In this sub-menu you select which drive letters you want to assign and the type of drive. Note that IDE0 = primary master, IDE1 = primary slave, IDE2 = secondary master and IDE3 = secondary slave.

There are several options for setting the drive type, including AUTOCONFIG PHYSICAL, AUTOCONFIG LBA along with several pre-defined drive settings. In most cases AUTOCONFIG LBA should be used on any newer hard drives greater than 512Mbytes. This allows the BIOS to query the drive for its optimum configuration.

3.2.1. ATA Flash Drive Setup

The IBC2901 contains an ATA Flash Drive socket, which allows the support of a Flash drive that appears to the application as an IDE drive. The ATA Flash Drive socket is to the primary IDE channel. Use the standard AUTOCONFIG LBA option to configure the IDE channel for an ATA Flash Drive.

3.2.2. CD-ROM Setup

No special setup is required in the BIOS to support a CD-ROM drive. The CD-ROM driver will examine the IDE channels, determine if a CD-ROM is present, and map a drive letter for the CD-ROM.

3.3. Saving to CMOS

After changing the various setup parameters select the WRITE TO CMOS AND EXIT menu to write the changes to the non-volatile CMOS memory. If you do not want to save your changes, select the EXIT WITHOUT CHANGING CMOS option.

4. Specifications

4.1. Compatibility

PCI Compatibility: PICMG 1.0, Version 2.0

4.2. Electrical

Parameter Operating Voltage	Specification	
	Minimum	**Maximum**
VCC = 5V	4.75 VDC	5.25 VDC
VCC = 3.3V	3.0 VDC	3.6 VDC
VCC = 12V (fansinks only)	11.0 VDC	13.0 VDC

Parameter Operating Current		Specification	
		Typical	**Maximum**
Single Celeron 366MHz, 32MB DRAM	VCC = 5V	2.7A	3.3A
	VCC = 3.3V	2.0A	2.4A
	VCC = 12V	.06A	.08A
Dual PIII 750MHz, 256MB DRAM, CDROM, Floppy	VCC = 5V	6.5A	7.9A
	VCC = 3.3V	3.1A	3.7A
	VCC = 12V	.120A	.160A

4.3. Mechanical

Parameter	Specification
Dimensions, Depth x Height	4.8in x 13.3in 121.9mm x 337.8mm
Dimensions, Width With CPU fansinks	1.3 in
Weight - Single Celeron, 8HP	20 oz

4.4. Environmental

Parameter	Specification
Operating Temperature, Ta	
Celeron 366MHz	0 to 59_C
Pentium III 750MHz	0 to 50_C
Storage Temperature, Ts	-40 to +85_C
Non-condensing Relative Humidity	Less than 95% at 40_C

4.5. Reliability

Parameter	Specification
MTBF CPU	TBD
MTBF FANSINK	
@ 50 _C	24.7 Years
@ 60 _C	12.3 Years
MTTR (Mean Time To Repair)	5 minutes

B

backplane: A device inside the chassis that contains slots, or sockets, for plugging in I/O cards or cables.

bidirectional parallel port: An eight-bit port that can be used as an input as well as an output device.

bus: One or more electrical conductors that transmit power or data to the various sections of a computer or any common pathway between hardware devices. A computer bus connects the CPU to its main memory and the control units of peripheral devices.

C

card cage: A cabinet or metal frame that holds printed circuit cards.

CMOS (Complementary Metal Oxide Semiconductor): A technology of arranging transistors on a semiconductor which uses very low power.

D

disk access LED: The LED located on the front control panel that indicates when the hard disk drive is active.

DRAM (Dynamic Random Access Memory): A type of computer memory that needs to be refreshed by a memory controller or it loses its information.

drive bay: Area in the chassis where drives are mounted.

E

electrostatic discharge (ESD): A sudden uncontrolled movement of accumulated electrical charge from one location to another. Voltage potentials and discharge currents associated with ESD can damage many types of electronic components used in computers. ESD prevention methods should always be employed when servicing computer hardware.

EMI (ElectroMagnetic Interference): Noise generated by the switching action of the power supply and other system components. Conducted EMI is interference generally conducted into the power line, and is normally controlled with a line filter. Radiated EMI is that portion that radiates into free space, one way to suppress it is by enclosing circuitry in a metal case.

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power.

expansion card: A printed circuit board that plugs into an expansion slot.

F

floppy drive: A device for reading information from or writing information to external, portable computer disks called floppy disks.

front control panel: The small panel on the front of the computer that usually contains one or more of the following: power switch, reset switch, Power ON LED, disk access LED, keyboard connector, status display, etc.

H

hard drive: A non-volatile data storage device. Hard drives magnetically store computer data on spinning internal disks.

I

IDE (Integrated Drive Electronics): A standard protocol for signalling and communicating with a hard drive, CD-ROM drive, or other peripheral device.

I/O card: A printed circuit board that plugs into an I/O slot.

I/O slot: A slot for plugging in additional I/O cards to expand the capability of a computer.

ISA: The original IBM/PC expansion bus standard released into the public domain by IBM.

K

keyboard connector: The connector through which keyboard signals are input to a computer.

kilobyte (KB): 1,024 bytes.

L

LED: Light Emitting Diode. Long-lasting light emitters usually used as indicators.

load board: A board having specific power load characteristics which are typically used for testing.

P

parallel port: I/O connector used to hook up a printer or other parallel interface device. The parallel port is usually a 25-pin female DB25 connector.

PCI(Peripheral Component Interconnect): A PC expansion bus standard maintained by the PCI Special Interest Group, a consortium of industrial partners.

port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

power good: A logic signal used to indicate that DC output from a PC power supply has stabilized. The power good line switches from 0 to +5 volts within one tenth to one half second after the power supply reaches normal voltage levels. Whenever output voltage is out of normal operating range for any reason, the power good signal goes back to zero.

power ON/diagnostic LED: The LED located on the front control panel that indicates that power is applied to the computer.

power supply: Electrical system that converts AC or DC source power into the lower level DC power required by the computer circuitry. In a personal computer, 3.3, +5, -5, +12 and -12 voltages are generated by the system power supply.

power switch: The power switch turns main source power ON/OFF to the computer. It is usually located on the front computer panel or the rear panel near the input power cable.

R

RAID (Redundant Arrays of Independent Disks): A storage technology using an array of two or more disks to redundantly store information. If one disk fails in a RAID array, the unit continues to function without loss of data.

RAM (Random Access Memory): The memory used to execute applications while your computer is turned ON. When you turn your computer OFF, all data stored in RAM is lost.

real-time clock (RTC): A periodic interrupt used to derive local time.

reset switch: Button or key that reboots the computer. All current activities are stopped and any data in memory is lost.

S

SCSI (Small Computer System Interface): A high speed, general purpose interface to storage devices.

SDR (Sensor Data Record): A record of data about a sensor. The full description of the contents of these records can be found in IPMI, version 1.0, section 28.1.

SEL (System Event Log): A non-volatile storage area and associated interfaces for storing system platform event information for later retrieval.

serial port: A two-channel port, one channel used for ”In” transmissions and one for ”Out” transmissions.

W

watchdog timer: A device that monitors CPU activity and resets the CPU when no activity is detected for a user specified period.

LIMITED WARRANTY

I-Bus/Phoenix warrants this product to be free of defects in material and workmanship for an initial period of two (2) years from date of delivery to the original purchaser from I-Bus/Phoenix.

During this period, I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, except as set forth in this warranty agreement.

I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, if the defect is related to the I-Bus/Phoenix manufactured product, such as power supply, backplanes, other chassis components, or CPUs. I-Bus/Phoenix is not liable for any defects in material or workmanship of any peripherals, products or parts which I-Bus/Phoenix does not design or manufacture. However, I-Bus/Phoenix will honor the original manufacturer's warranty for these products.

I-Bus/Phoenix will analyze the defective component and the customer will be charged in the following instances:

- No problem found: $75 (U.S. dollars).
- Damage: parts and labor at $75 per hour with a $100 minimum charge (U.S. dollars). Receipt of damaged goods voids the I-Bus/Phoenix warranty.

Repair parts and replacement products will be furnished on an exchange basis and will be either new or reconditioned. All replacement parts and products shall become the property of I-Bus/Phoenix, if such parts or products are provided under this warranty agreement. In the event a defect is not related to the I-Bus/Phoenix manufactured product, I-Bus/Phoenix shall repair or replace the defective parts at purchaser's cost and deliver the defective parts to the purchaser.

This Limited Warranty shall not apply if the product has been misused, carelessly handled, defaced, modified or altered, or if unauthorized repairs have been attempted by others.

The above warranty is the only warranty authorized by I-Bus/Phoenix and is in lieu of any implied warranties, including implied warranty of merchantability and fitness for a particular purpose.

In no event will I-Bus/Phoenix be liable for any such damage as lost business, lost profits, lost savings, downtime or delay, labor, repair or material cost, injury to person or property or any similar or dissimilar consequential loss or damage incurred by purchaser, even if I-Bus/Phoenix has been advised of the possibility of such losses or damages.

In order to obtain warranty service, the product must be delivered to the I-Bus/Phoenix facility, or to an authorized I-Bus/Phoenix service representative, with all included parts and accessories as originally shipped, along with proof of purchase and a Returned Merchandise Authorization (RMA) number.

The RMA number is obtained, in advance, from I-Bus/Phoenix Customer Service Department and is valid for 30 days. The RMA number must be clearly marked on the exterior of the original shipping container or equivalent. Purchaser will be responsible and liable for any missing or damaged parts. Purchaser agrees to pay shipping charges one way, and to either insure the product or assume the liability for loss or damage during transit. Ship to:

I-Bus/Phoenix
ATTENTION: RMA REPAIR DEPT.
RMA ####
8888 Balboa Avenue
San Diego, CA 92123

This page was intentionally left blank

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

WARNING: This equipment has been tested and found to comply with the limits for a Class "A" digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This product was FCC verified under test conditions that included the use of shielded I/O cables and connectors between system components. To be in compliance with FCC regulations, the user must use shielded cables and connectors and install them properly.

This page was intentionally left blank