2801

CompactPCI Processor Board

User's Guide

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1. Introduction

1.1 Lithium Battery Replacement

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Ersatz rur durch denselben oder einen vom Hersteller empfohlenengleichwertigen Typ. Entsorgung gerbrauchter Batterien noch Angaben Herstellers.

1.2 Product Description

The 2801 is a single-slot 6U CompactPCI® system master designed to support a single or dual Mobile Intel® Pentium® III Processor-M. The 2801 supports DDR DRAM. Additional features include dual 10/100 Base-TX Ethernet channels, an embedded SCSI controller, SVGA video, and 32-bit PMC expansion. The 2801 also supports a full set of standard PC peripherals: IDE, floppy, USB, serial, parallel, mouse, and keyboard. Additional industrial features include battery-backed real time clock, CPU temperature monitor, board temperature monitor, supply voltage monitors, and a watchdog timer.

The 2801 front panel connectors include SVGA video, dual 10/100-BaseTX Ethernet, USB, keyboard/mouse, and PMC expansion. The 2801 also directs several peripherals to the CompactPCI connectors for rear panel cabling. These interfaces include SVGA Video, dual 10/100-BaseTX Ethernet, SCSI, USB, keyboard, mouse, PMC, dual serial, parallel, IDE, and floppy.

1.3 Standard Features

- 6U (160mm x 233.5mm) x 4HP (single slot) CompactPCI® form factor
- Single or dual Mobile Intel® Pentium® III Processor-M at 800MHz
- 512Kbytes integrated L2 cache on Mobile Tualatin processors
- Up to 1Gbtyes of DDR SDRAM with a single-slot card height
- Up to 2Gbytes of DDR SDRAM with a double-slot card height
- 512 Kbytes of Flash for System BIOS
- SVGA video support up to 1600x1200x64K (front & rear panel)
- Dual 10/100 Base-TX Ethernet channels (front & rear panel)
- Ultra SCSI-3 controller supports 160 MB/s data transfer
- 32-bit PCI Mezzanine Card (PMC) Expansion (front & rear panel)
- 32-bit/64-bit 33MHz/66MHz CompactPCI Bus (PICMG 2.0 R3.0)
- Packet Switching Backplane compliant (PICMG 2.16 Draft 0.9.1)
- IPMI System Management option (PICMG 2.9 R1.0)
- Battery-Backed CMOS and Real Time Clock
- Selectable stand-alone operation in or out of CompactPCI chassis
- Supply voltage and temperature sensors
- Watchdog timer
- Standard PC peripherals/O supported:
- Ultra IDE, floppy (mezzanine & rear panel)
- USB, mouse, keyboard (front & rear panel)
- Serial, parallel (rear panel)
- Front panel reset push buttons
- Microsoft Windows® or Red Hat Linux Compatible

1.4 Functional Blocks

A functional block diagram for the 2801 is shown in Figure 1-1. The major functional blocks are discussed in detail below.

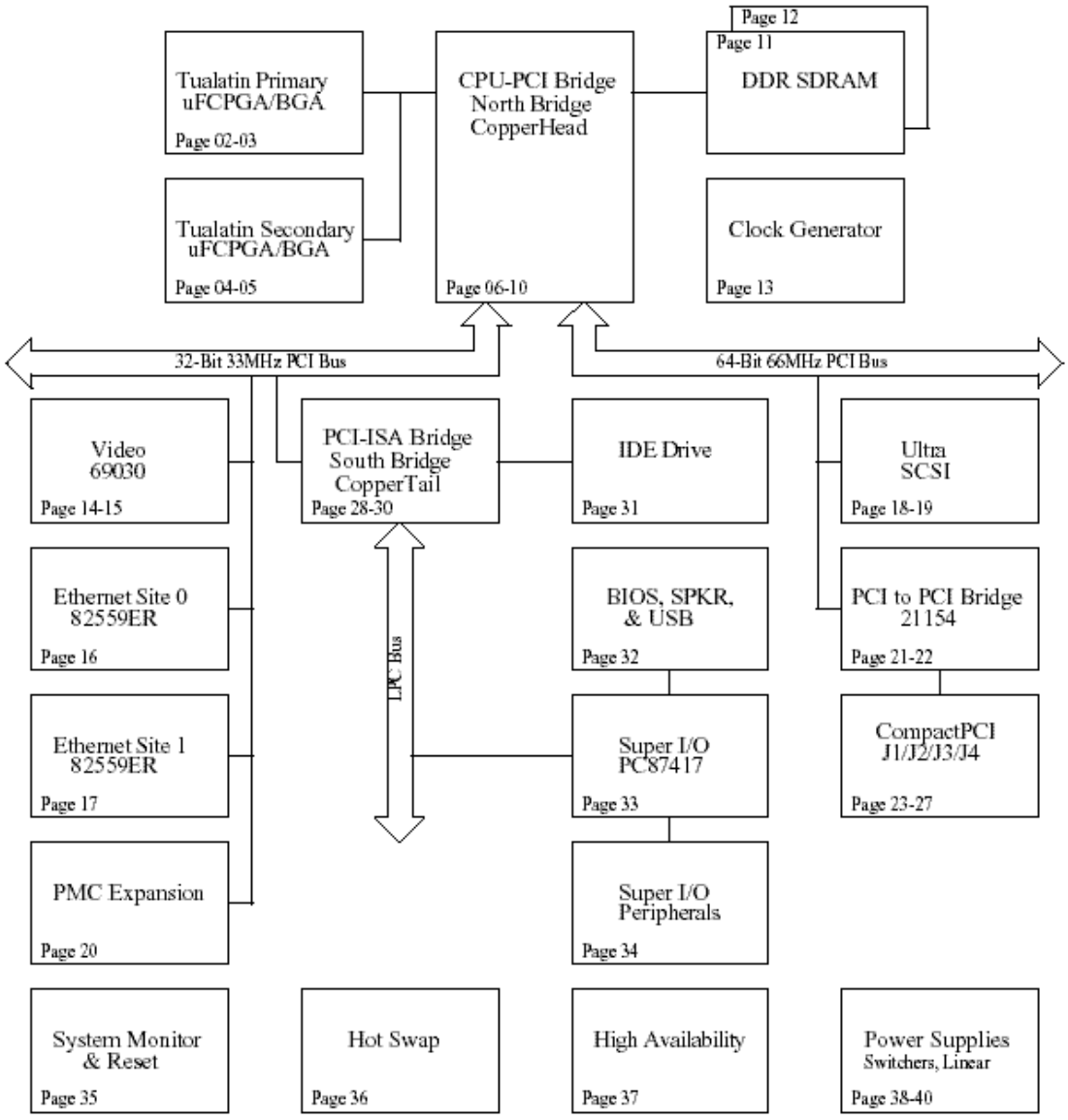

Figure 1-1. 2801 Functional Block Diagram

1.4.1 Processor Architecture

The 2801 CPU architecture supports the Mobile Intel Pentium III Processor – M in both single and dual processor configurations. The processor includes a 512-Kbyte full-speed cache and a 133MHz system bus speed. Additional features include dynamic power management and an internal temperature sensor for monitoring processor temperature.

1.4.2 System DRAM

The 2801 includes two 168-pin DDR DIMM sockets. Each of these sockets support PC1600/PC2100 modules in densities up to 256 Mbytes. Fully populated, this adds up to 512 Mbytes of system DRAM.

1.4.3 BIOS Flash

The system BIOS is contained in a single 512 Kbyte Flash loaded into a 32-pin PLCC socket. The ability to modify the contents of the Flash can be disabled through the removal of a series zero ohm resistor on the write enable line.

1.4.4 SVGA Video

The 2801 includes an Intel 69030 Advanced Graphics Port SVGA video controller with 4Mbytes of video memory. The video controller supports display resolutions up to 1600X1200X64K color in single display mode.

The SVGA Video is available through both the front panel and the rear panel. The front panel SVGA connector is an industry standard 15-pin D-shell configuration compatible with standard desktop monitors.

1.4.5 Dual 10/100 Base-TX Ethernet

The 2801 includes two Intel 82559ER 10/100 Base-TX Ethernet controllers. The Ethernet controller is a 32-bit PCI device that includes both the Media Access Controller (MAC) and the Physical Layer Controller (PHY). The MAC supports 10 Mbps and 100 Mbps operation compliant with the IEEE 802.3 standard. The PHY supports 10 Base-T and 100 Base-TX operation compliant with the IEEE 802.3 standard.

The 10/100 Base-TX Ethernet is available through both the front panel and the rear panel. The front panel Ethernet connectors are an industry standard 8-pin RJ45. Each connector includes two light emitting diodes (LEDs). The green LED indicates LINK/ACTIVITY and the yellow LED indicates LINK SPEED. The LINK/ACTIVITY LED in on when a link is established and blinks when there is activity. The LINK SPEED LED is off for 10Mbit operation and lights for 100Mbit operation.

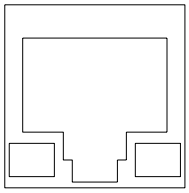

Figure 1-2. Ethernet Status LEDs

1.4.6 SCSI Controller

The 2801 includes an LSI 53C1000 Ultra160 SCSI controller. This controller supprts wide synchronous transfer rates up to 160 MBps using an LVD SCSI bus. It supports Fast SCSI, Ultra SCSI, Ultra2 SCSI, and Ultra160 SCSI.

The SCSI signals are available on a 68-pin SCSI connector (J3) of the 2703 rear panel.

1.4.7 IDE Drives

The 2801 supports both a primary and a secondary IDE channel. The IDE controller supports Ultra ATA/100/66/33 operating modes with independent timings for up to four drives.

The primary IDE channel is available through the rear panel. The secondary IDE channel is routed to a 50-pin 2mm header. The header is designed to accept an optional mezzanine board for supporting an IDE hard drive and a Compact Flash while still maintaining a single slot (4HP) board height. The optional mezzanine board is the 16010.

1.4.8 PMC Expansion

The PCI Mezzanine Card (PMC) defines the connector pin assignments and mechanical dimensions for a mezzanine board based on a PCI interface. The PMC architecture is compliant with IEEE 1386 for a 32-bit implementation. The electrical interface includes three Molex 71439-2164 (or equivalent) connectors.

The front panel of the PMC board is available through the 2801 front panel. The user I/O connector of the PMC is mapped to the 2801 rear panel to support rear panel accessibility of PMC features such as SCSI.

1.4.9 CompactPCI Interface

The 2801 is electrically and mechanically compatible with the PICMG 2.0 R3.0 CompactPCI Specification, and based on the industry standard Eurocard 6U form factor (233mm X 160mm). The 2801 functions as a peripheral master in a CompactPCI architecture with one system slot and one or more peripheral slots. The 2801 supports both 64-bit and 32-bit transfers operating at 66 MHz or 33 MHz. 2801 also supports the PICMG 2.16 Draft 0.9.1 Packet Switching Backplane Specification.

A jumper setting allows the 2801 to operate in either a system slot or a peripheral slot without the use of the CompactPCI bus. This operating mode is useful for systems that have several 2801 processors communicating over a medium other than the CompactPCI bus.

The 2801 uses the industry standard Intel 21555 non-transparent bridge. The 2801 supports backplane VI/O voltages of either 3.3V or 5V.

1.4.10 Super I/O

The National Semiconductor PC87417 Super I/O includes two serial ports, an IEEE1284 parallel port, a floppy disk controller, a keyboard controller, a mouse controller, an SMBus controller, and a real time clock. A standard CR2032 coin cell battery provides battery-backup for the real time clock. The battery is located in a socket to facilitate replacement. The minimum battery life is 5 years.

The serial ports support standard RS-232 signal levels at baud rates up to 115 Kbaud. The serial ports, parallel port, and floppy disk interfaces are available through the rear panel. The keyboard and mouse interfaces are combined into a single 6-pin MiniDIN connector that is available through the front panel. Both interfaces are independently available through the rear panel. The SMBus controller and the real time clock are used locally.

1.4.11 Hardware Monitor

A National Semiconductor LM87 Hardware Monitor provides CPU temperature, supply voltage, and fan speed monitoring.

1.4.12 Watchdog Timer

A watchdog timer optionally monitors system operation to be sure that the application software is executing as designed. The watchdog timer generates a hardware reset if it is not accessed by the application software within the minimum time interval. Chapter 2 details the watchdog timer operation.

1.4.13 DC/DC Converter

The 2801 includes DC/DC converters for supplying the core operating voltage to the processors. The Linear Technology LTC1709 2-phase synchronous step-down current mode switching controller meets the Intel VRM specification and supplies voltages ranging from 0.925V to 2.00V

1.4.14 IPMI Expansion

The 2801 includes an expansion site for an optional system management controller board. The PICMG 2.8 R1.0 compliant board supports both BMC (Baseboard Management Controller) and PM (Peripheral Management Controller) configurations. For more detail, see Platform Management IBUS # 101842.

2. Configuration and Installation

2.1 Memory and I/O Mapping

There are several memory and I/O devices local to the 2801. There are also expansion sites for adding memory and I/O resources. The address maps for these devices are shown in Table 2-1 below.

Memory Space	Memory Address (hex)	Description
768M - 4G	30000000 – FFFFFFFF	Available
1M - 768M	00100000 – 2FFFFFFF	System Memory
896K - 1024K	000E0000 – 000FFFFF	System BIOS
800K - 896K	000C8000 – 000DFFFF	BIOS Expansion
768K - 800K	000C0000 – 000C7FFF	VGA BIOS
640K - 768K	000A0000 – 000BFFFF	VGA DRAM
0K - 640K	00000000 – 0009FFFF	System DRAM

Table 2-1: Memory Map

I/O Address (hex)	Device
40AE	General Purpose Outputs
40A6	General Purpose Inputs
0CF8 – 0CFF	PCI Configuration
04D0 – 04D1	Interrupt Controller
0480 – 048F	DMA Page
03F8 – 03FF	COM1
03F6 – 03F7	Primary IDE
03F0 – 03F7	Floppy & IDE
0376 – 0377	Secondary IDE
02F8 – 02FF	COM2
01F0 – 01F7	Primary IDE
0170 – 0177	Secondary IDE
00F0 – 00F1	Coprocessor
00C0 – 00DF	DMA Controller
00B2 – 00B3	Power Management
00A0 – 00A1	Interrupt Controller
0092	Port 92 Control
0080 – 008F	DMA Page
0070 – 0073	Real Time Clock
0060 – 0064	Keyboard Controller
0040 – 0043	Timer/Counters
002E – 002F	Super I/O Configuration
0020 – 0021	Interrupt Controller
0000 – 000F	DMA Controller

Table 2-2: I/O Map

2.2 PCI Device Mapping

The 2801 includes the PCI device mapping listed in Table 2-3 below.

Bus Number	Device Number	Fcn Number	Vendor ID	Device ID	Description
					Micron North Bridge
00	07	00	1344	3470	Host Bridge
00	07	02	1344	3472	IDE
00	07	03	1344	3473	USB
00	14	00	1344	3330	Micron South Bridge
					Intel 82559
00	0B	00	8086	1209	Ethernet
00	0C	00	8086	1209	Ethernet 1
					Ethernet 2
					Intel 82546
00	08	00	8086	1010	Ethernet
00	08	01	8086	1010	Ethernet 3
					Ethernet 4
00	0E	00	102C	0C30	Intel SVGA Video
01	0B	00	8086	B555	Intel CPCI Bridge
02	09	XX	XXX	XXX	CompactPCI Peripheral Slot 1
02	0A	XX	XXX	XXX	CompactPCI Peripheral Slot 2
02	0B	XX	XXX	XXX	CompactPCI Peripheral Slot 3
02	0C	XX	XXX	XXX	CompactPCI Peripheral Slot 4
02	0D	XX	XXX	XXX	CompactPCI Peripheral Slot 5
02	0E	XX	XXX	XXX	CompactPCI Peripheral Slot 6
02	0F	XX	XXX	XXX	CompactPCI Peripheral Slot 7

Table 2-3: PCI Device Map

2.3 Interrupt Mapping

The 2801 includes the standard PC-compatible interrupt architecture for monitoring 15 interrupt inputs. The interrupt sources are shown in the following Table 2-4. PCI interrupts are level sensitive and are shared between on-board PCI devices and CompactPCI peripherals.

Interrupt	Function
0	System Timer
1	Keyboard
2	Slave Interrupt Controller
3	COM2 Serial
4	COM1 Serial
5	PCI
6	Floppy
7	LPT
8	Real Time Clock
9	PCI
10	PCI
11	PCI
12	Mouse
13	Coprocessor
14	IDE Primary
15	IDE Secondary

Table 2-4: Interrupt Sources

2.4 Parallel I/O

The 2801 includes parallel I/O bits coming from the Coppertail South Bridge for controlling and monitoring various functions. Input bits are located at port 40A6h and output bits are located at port 40AEh. Table 2-5 details the operation for each bit. See the Micron Copperhead data sheet for more information on programming these registers. Do not re-program RESERVED bits.

Port	Bit	Description
40A6h (Inputs)	0	Power Supply DEG (J2 CompactPCI)
	1	Power Supply FAIL (J2 CompactPCI)
	2	Fan 0 Failure Status (J4 CompactPCI)
	3	Fan 1 Failure Status (J4 CompactPCI)
	4	Watchdog Strobe Status
	5	Hot Swap LED Status
	6	User LED Status
	7	Reserved
	8	GA0 – Geographic Address 0 (J2 CompactPCI)
	9	GA1 – Geographic Address 1 (J2 CompactPCI)
	10	GA2 – Geographic Address 2 (J2 CompactPCI)
	11	GA3 – Geographic Address 3 (J2 ComapctPCI)
	12	GA4 – Geographic Address 4 (J2 CompactPCI)
	13-15	Reserved
40Aeh (Outputs)	0-3	Reserved
	4	Watchdog Strobe
	5	User LED Control
	6	Hot Swap LED Control
	7-15	Reserved

Table 2-5: Board Specific I/O

2.5 Watchdog Control

The 2801 provides watchdog timer capability using the Dallas Semiconductor DS1819A reset monitor. The watchdog strobe circuit consists of a free running clock, gated with an enable bit, and connected to the strobe input of the DS1819A. When the enable bit is low (40AEh bit 4 is written to 0) the clock will strobe the watchdog. When this bit is high the clock is shut off and the watchdog timer activated. Once the watchdog is activated, the enable bit must be taken back low within 1.2 seconds to reset the timer. Following is a sample routine for controlling the watchdog timer.

ACTIVATE WATCHDOG

```
IN      AL,40A6h
OR      AL,10h
OUT     40AEh,AL
```

STROBE WATCHDOG

```
IN      AL,40A6h
AND     AL,EFh
OUT     40AEh,AL
OR      AL,10h
OUT     40AEh,AL
```

2.6 User LED

The 2801 contains a user LED on the frontplate. The LED is programmed through bit 6 of port 40A6h.

2.7 Clearing CMOS

The Super I/O controller battery backed memory contains the 2801 setup information. To clear this information and reset the board to the BIOS defaults follow the below steps:

1. Turn off system power.
2. Move jumper W9 from position 1-2 to position 2-3 and then back.

The battery supplied with the 2801 is a standard CR2032 coin cell rated for 210mAH. The battery life is approximately 70K hours (8 years).

2.8 BIOS Update

The BIOS for the 2801 is located in a 512 Kbyte Flash memory located in the 32-pin PLCC socket. Upgrade the BIOS using the FLASH.EXE utility. Contact I-Bus for the latest BIOS and Flash utility. Update the BIOS using the steps listed below.

1. Power the 2801 and boot to a DOS prompt.
2. Type FLASH.EXE xxxxx.BIN (where xxxxx.BIN is the new BIOS image binary file).
3. Power cycle the computer.

2.9 Ethernet Configuration

The 2801 supports the two 10/100 Base-TX Ethernet channels through either the front panel connectors or the rear panel connectors using the optional 2703 or 2704. Isolation jumper settings are required to avoid signal degradation.

Ethernet Channel 1 Configuration	
Front Panel (J6)	Install plugs in position 2-3 of jumpers W1-W4
Rear Panel	Install plugs in position 1-2 of jumpers W1-W4

Ethernet Channel 2 Configuration	
Front Panel (J8)	Install plugs in position 2-3 of jumpers W5-W8
Rear Panel	Install plugs in position 1-2 of jumpers W5-W8

Table 2-6: 10/100 Base-TX Ethernet Routing

2.10 Interface Connectors

The 2801 connector pin assignments and signal descriptions are included in the following sections.

- J1: CompactPCI Backplane J5
- J2: Keyboard/Mouse
- J3: USB
- J4: CompactPCI Backplane J4
- J5: Video
- J6: Ethernet Channel 0
- J7: IMPI Expansion
- J8: Ethernet Channel 1
- J9: DRAM 1 Socket
- J10: DRAM 2 Socket
- J11: CompactPCI Backplane J3
- J12: PMC Expansion
- J13: PMC Expansion
- J14: CompactPCI Backplane J2
- J15: PMC Expansion
- J16: Battery Socket
- J17: CompactPCI Backplane J1
- J18: Hot Swap Ejector
- J19: Speaker
- J20: IDE/Floppy Expansion

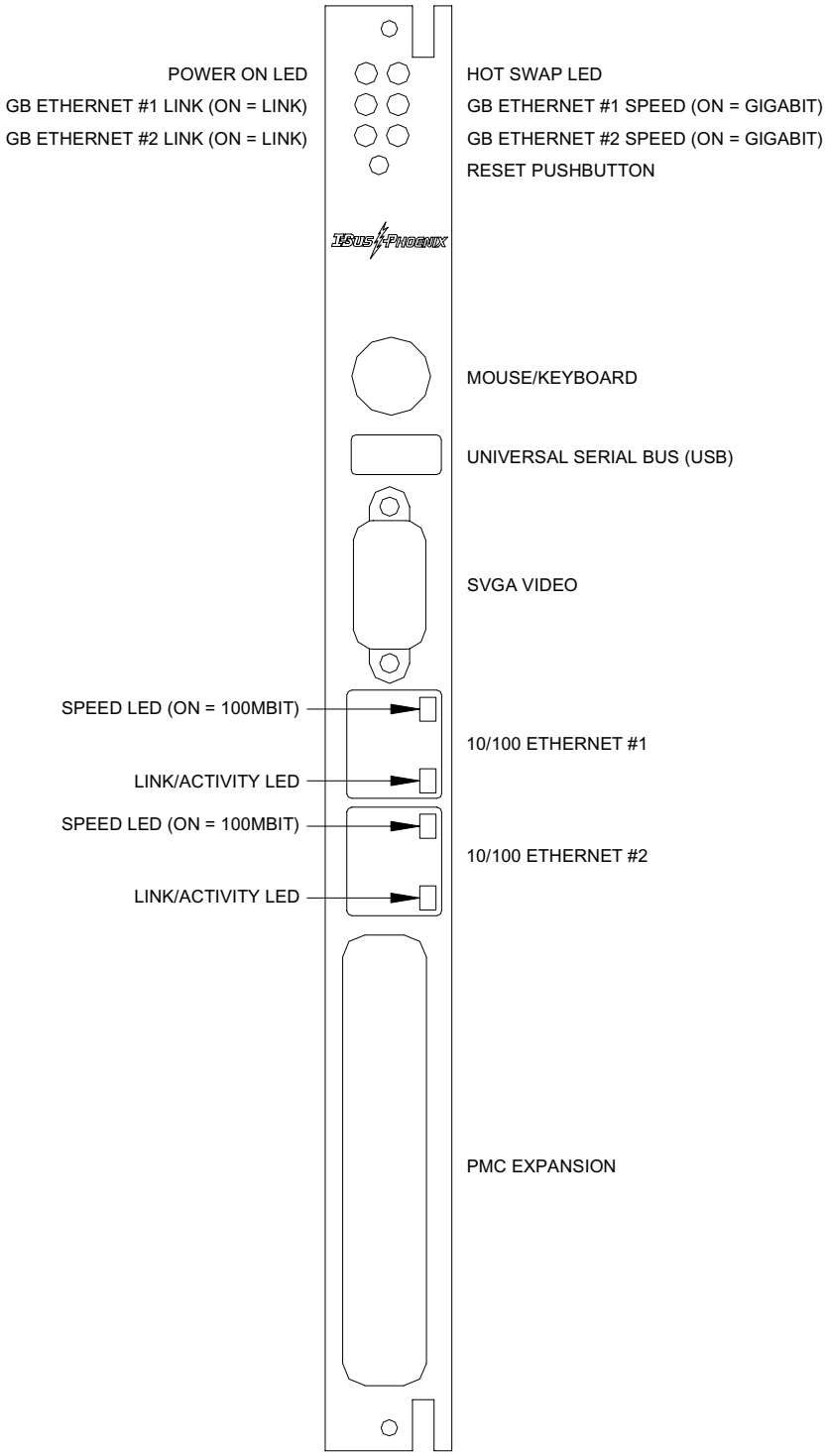

Figure 2-1: Front Panel

2.10.1 J5 CompactPCI Connector (J1)

This connector contains the primary IDE, floppy, USB, COM1, COM2, keyboard, mouse, SVGA video, speaker, and two 10/100 Base-TX Ethernet channels.

Pin	A	B	C	D	E	F
22	HPD0	HPD1	HPD2	HPD3	HPD4	GND
21	HPD5	HPD6	HPD7	HPD8	HPD9	GND
20	HPD10	HPD11	HPD12	HPD13	HPD14	GND
19	HPD15	HPA0	HPA1	HPA2	N/C	GND
18	N/C	HPCS1#	HPCS3#	HPIRDY	N/C	GND
17	HPIOR#	HPIOW#	HPDRQ	HPDAK#	N/C	GND
16	HPDSP#	HPDIAG#	HPRST#	HPIR15	N/C	GND
15	FDCHG#	5V	5V	3.3V	3.3V	GND
14	FRDAT#	FWP#	FTRK0#	FINDX#	FHDSL#	GND
13	FSTEP#	FDNSL#	FDIR#	FWGAT#	FWDAT#	GND
12	FDS0#	FDS1#	FMTR0#	FMTR1#	FDR1#	GND
11	5V	5V	GND	3.3V	3.3V	GND
10	U0DP	S1TXD	S1RTS#	S1DTR#	S1DCD#	GND
9	U0DN	S1RXD	S1CTS#	S1DSR#	S1RI#	GND
8	U1DP	S0TXD	S0RTS#	S0DTR#	S0DCD#	GND
7	U1DN	S0RXD	S0CTS#	S0DSR#	S0RI#	GND
6	KDAT	KCLK	GND	MDAT	MCLK	GND
5	5V	5V	GND	3.3V	3.3V	GND
4	VBLU	VGRN	VRED	VHSYN	VSYNC	GND
3	VDAT	VCLK	GND	N/C	SPKR	GND
2	E1TXN	E1TXP	GND	E0RXN	E0RXP	GND
1	E1RXN	E1RXP	GND	E0TXN	E0TXP	GND

Table 2-7: J1 Connector Pin Assignment

2.10.2 Keyboard/Mouse Connector (J2)

The frontplate keyboard connector is an industry standard 6-pin MiniDIN female connector. The Mouse signals have also been mapped to this connector to allow use of a splitter cable for both keyboard and mouse support.

Pin Number	Signal
1	Keyboard Data
2	Mouse Data
3	GND
4	Fused 5V
5	Keyboard Clock
6	Mouse Clock

Table 2-8: J2 Pin Assignments

2.10.3 USB Connector (J3)

The frontplate USB connector is an industry standard 4-pin USB connector.

Pin Number	Signal

1	Fused 5V
2	USB-
3	USB+
4	GND

Table 2-9: J3 Pin Assignments

2.10.4 J4 CompactPCI Connector (J4 - Not Loaded)

This connector contains the LPT parallel port, and fan monitoring signals. This connector is generally not loaded for support of backplanes that map other functions, such as the H110 bus, to the CompactPCI J4 connector pins.

Pin	A	B	C	D	E	F
25	N/C	N/C	N/C	N/C	N/C	GND
24	N/C	N/C	N/C	N/C	N/C	GND
23	N/C	N/C	N/C	N/C	N/C	GND
22	N/C	N/C	N/C	N/C	N/C	GND
21	N/C	N/C	N/C	N/C	N/C	GND
20	N/C	N/C	N/C	N/C	N/C	GND
19	N/C	N/C	N/C	PD0	PD1	GND
18	PD2	PD3	PD4	PD5	PD6	GND
17	PD7	PPE	PBUSY	PSLCT	PERR#	GND
16	PACK#	PSLIN#	PINIT#	PALF#	PSTB#	GND
15	5V	5V	GND	3.3V	3.3V	GND
14	KEY AREA					GND
13						GND
12						GND
11	N/C	N/C	N/C	N/C	N/C	GND
10	N/C	N/C	N/C	N/C	N/C	GND
9	N/C	N/C	N/C	N/C	N/C	GND
8	N/C	N/C	N/C	N/C	N/C	GND
7	N/C	N/C	N/C	N/C	N/C	GND
6	5V	5V	GND	3.3V	3.3V	GND
5	N/C	N/C	N/C	F0FAIL#	F1FAIL#	GND
4	N/C	N/C	N/C	N/C	N/C	GND
3	N/C	N/C	N/C	N/C	N/C	GND
2	N/C	N/C	N/C	N/C	N/C	GND
1	N/C	N/C	N/C	N/C	N/C	GND

Table 2-10: J4 Connector Pin Assignment

2.10.5 Video Connector (J5)

The frontplate video connector is an industry standard 15-pin HD DB15 female connector.

Pin Number	Signal
1	RED
2	GREEN
3	BLUE
4	N/C
5	GND
6	GND
7	GND
8	GND
9	Fused 5V
10	GND
11	N/C
12	SDAT
13	HSYNC
14	VSYNC
15	SCLK

Table 2-11: J5 Pin Assignments

2.10.6 Front Panel Ethernet (J6/J8)

The front panel Ethernet connectors use industry standard 8-pin RJ45's.

Pin Number	Signal
1	TX+
2	TX-
3	RX+
4	Termination
5	Termination
6	RX-
7	Termination
8	Termination

Table 2-12: J6/J8 Pin Assignments

2.10.7 IPMI Expansion (J7)

The IPMI expansion connector supports an optional I-Bus mezzanine board with the following pin assignment.

Pin	Signal	Pin	Signal
1	VCCIPMB	2	GND
3	SCL	4	BASCL
5	SDA	6	BASDA
7	COM2EN#	8	BALERT#
9	LAD0	10	BBSCL
11	LAD1	12	BBSDA
13	LAD2	14	GEOADD0
15	LAD3	16	GEOADD1
17	LFRAME#	18	GEOADD2
19	PCIRST#	20	GEOADD3
21	TXD	22	GEOADD4
23	RXD	24	LOCRST#
25	LCLK	26	SWSTAT
27	GND	28	SYSEN

Table 2-13: J7 Pin Assignments

2.10.8 DIMM Sockets (J9/J10)

The two DIMM memory sockets accept industry standard 168-pin EDO DIMM memory modules. The DIMM modules must be less than 0.95” tall to prevent the 2801 from extending into the next board slot. The modules must be unbuffered PC2100 devices.

2.10.9 J3 CompactPCI Connector (J11)

This connector contains the SCSI signals and the PMC user I/O signals.

Pin	A	B	C	D	E	F
19	N/C	N/C	N/C	N/C	N/C	GND
18	LPADAP PMC15	LPADAN PMC13	GND	LPADCP PMC11	LPADCN PMC9	GND
17	LPADBP PMC16	LPADBN PMC14	GND	LPADDP PMC12	LPADDN PMC10	GND
16	LPBDAP PMC7	LPBDAN PMC5	GND	LPBDCP PMC3	LPBDCN PMC1	GND
15	LPBDBP PMC8	LPBDBN PMC6	GND	LPBDDP PMC4	LPBDDN PMC2	GND
14	5V	5V	3.3V	3.3V	3.3V	GND
13	SD01P	SD15P	SD14P	SD13P	SD12P	GND
12	SD01N	SD15N	SD14N	SD13N	SD12N	GND
11	SDP4P	SD03P	SD02P	SD01P	SD00P	GND
10	SDP4N	SD03N	SD02N	SD01N	SD00N	GND
9	SD06N	SD06P	Reserved	SD05N	SD05P	GND
8	SDP0N	SDP0P	GND	SD07N	SD07P	GND
7	Reserved	DIFFSEN	GND	SATNN	SATNP	GND
6	SACKN	SACKP	GND	SBSYN	SBSYP	GND
5	SMSGN	SMSGP	GND	SRSTN	SRSTP	GND
4	SCDN	SCDP	GND	SSELN	SSELP	GND
3	SION	SIOP	GND	SREQN	SREQP	GND
2	SD09N	SD09P	GND	SD08N	SD08P	GND
1	SD11N	SD11P	GND	SD10N	SD10P	GND

Table 2-14: J11 Connector Pin Assignment

2.10.10 PMC Connectors (J12/J13/J15)

The PMC connectors are fully compliant with the IEEE 1386 specification for a 32-bit implementation. The 2801 uses a Molex 71439-0164 connector on the baseboard to support standard 10mm PMC spacing. Universal or 5V PMC modules are supported. The signal assignments on the User I/O connector are made with support of industry standard SCSI PMC modules to permit rear panel connection.

Pin	Signal	Pin	Signal
1	N/C	2	N/C
3	GND	4	INTA#
5	INTB#	6	INTC#
7	N/C	8	5V
9	INTD#	10	N/C
11	GND	12	N/C
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	5V
19	5V	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	CBE3#
27	AD22	28	AD21
29	AD19	30	5V
31	5V	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	5V
39	GND	40	LOCK#
41	N/C	42	N/C
43	PAR	44	GND
45	5V	46	AD15
47	AD12	48	AD11
49	AD09	50	5V
51	GND	52	CBE0#
53	AD06	54	AD05
55	AD04	56	GND
57	5V	58	AD03
59	AD02	60	AD01
61	AD00	62	5V
63	GND	64	5V PULLUP

Table 2-15: J12 Pin Assignments

Pin	Signal	Pin	Signal
1	N/C	2	N/C
3	N/C	4	N/C
5	N/C	6	GND
7	GND	8	N/C
9	N/C	10	N/C
11	5V	12	3.3V
13	RST#	14	GND
15	3.3V	16	GND
17	N/C	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V
25	IDSEL	26	AD23
27	3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	CBE2#
33	GND	34	N/C
35	TRDY#	36	3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	3.3V	42	SERR#
43	CBE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD08	50	3.3V
51	AD07	52	N/C
53	3.3V	54	N/C
55	N/C	56	GND
57	N/C	58	N/C
59	GND	60	N/C
61	5V PULLUP	62	3.3V
63	GND	64	N/C

Table 2-16: J13 Pin Assignments

Pin	Signal	Pin	Signal
1	J11.E13/SD12P	2	J11.E12/SD12N
3	J11.D13/SD13P	4	J11.D12/SD13N
5	J11.C13/SD14P	6	J11.C12/SD14N
7	J11.B13/SD15P	8	J11.B12/SD15N
9	J11.A13/SDP1P	10	J11.A12/SDP1N
11	J11.E11/SD00P	12	J11.E10/SD00N
13	J11.D11/SD01P	14	J11.D10/SD01N
15	J11.C11/SD02P	16	J11.C10/SD02N
17	J11.B11/SD03P	18	J11.B10/SD03N
19	J11.A11/SD04P	20	J11.A10/SD04N
21	J11.E9/SD05P	22	J11.D9/SD05N
23	J11.B9/SD06P	24	J11.A9/SD06N
25	J11.E8/SD07P	26	J11.D8/SD07N
27	J11.B8/SDP0P	28	J11.A8/SDP0N
29	N/C	30	N/C
31	J11.C9/DIFSEN	32	N/C
33	J11.E7/TERMPWR	34	J11.D7/TERMPWR
35	N/C	36	N/C
37	J11.B7/SATNP	38	J11.A7/SATNN
39	N/C	40	N/C
41	J11.E6/SBSYP	42	J11.D6/SBSYN
43	J11.B6/SACKP	44	J11.A6/SACKN
45	J11.E5/SRSTP	46	J11.E6/SRSTN
47	J11.B5/SMSGP	48	J11.A5/SMSGN
49	J11.E4/SSELP	50	J11.D4/SSELN
51	J11.B4/SCDP	52	J11.A4/SCDN
53	J11.E3/SREQP	54	J11.D3/SREQN
55	J11.B3/SIOP	56	J11.A3SION
57	J11.E2/SD08P	58	J11.D2/SD08N
59	J11.B2/SD09P	60	J11.A2/SD09N
61	J11.E1/SD10P	62	J11.D1/SD10N
63	J11.B1/SD11E	64	J11.A1/SD11N

Table 2-17: J15 Pin Assignments

2.10.11 J2 CompactPCI Connector (J14)

This connector contains the 64-bit PCI bus signals.

Pin	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	N/C	GND	N/C	N/C	N/C	GND
20	N/C	GND	N/C	GND	N/C	GND
19	GND	GND	SMBDAT	SMBCLK	ALERT#	GND
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	N/C	N/C	N/C	GND
16	N/C	N/C	DEG#	GND	N/C	GND
15	N/C	GND	FAIL#	N/C	N/C	GND
14	AD35	AD34	AD33	GND	AD32	GND
13	AD38	GND	VIO	AD37	AD36	GND
12	AD42	AD41	AD40	GND	AD39	GND
11	AD45	GND	VIO	AD44	AD43	GND
10	AD49	AD48	AD47	GND	AD46	GND
9	AD52	GND	VIO	AD51	AD50	GND
8	AD56	AD55	AD54	GND	AD53	GND
7	AD59	GND	VIO	AD58	AD57	GND
6	AD63	AD62	AD61	GND	AD60	GND
5	CBE5#	64EN#	VIO	CBE4#	PAR64	GND
4	VIO	N/C	CBE7#	GND	CBE6#	GND
3	N/C	GND	N/C	N/C	N/C	GND
2	N/C	N/C	SYSEN#	N/C	N/C	GND
1	N/C	GND	N/C	N/C	N/C	GND

Table 2-18: J14 Connector Pin Assignment

2.10.12 Battery Socket (J16)

The battery supplied with the 2801 is a standard CR2032 coin cell rated for 210mAH. The average battery life is 70,000 hours or about eight years.

2.10.13 J1 CompactPCI Connector (J17)

This connector contains the 32-bit PCI bus signals.

PIN	A	B	C	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD1	5V	VIO	AD0	ACK64#	GND
23	3.3V	AD4	AD3	5V	AD2	GND
22	AD7	GND	3.3V	AD6	AD5	GND
21	3.3V	AD9	AD8	M66EN	CBE0#	GND
20	AD12	GND	VIO	AD11	AD10	GND
19	3.3V	AD15	AD14	GND	AD13	GND
18	SERR#	GND	3.3V	PAR	CBE1#	GND
17	3.3V	IPMBSC	IPMBSD	GND	PERR#	GND
16	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	BSEL	TRDY#	GND
14	KEY AREA					GND
13						GND
12						GND
11	AD18	AD17	AD16	GND	CBE2#	GND
10	AD21	GND	3.3V	AD20	AD19	GND
9	CBE3#	IDSEL	AD23	GND	AD22	GND
8	AD26	GND	VIO	AD25	AD24	GND
7	AD30	AD29	AD28	GND	AD27	GND
6	REQ#	GND	3.3V	CLK	AD31	GND
5	N/C	N/C	RST#	GND	GNT#	GND
4	IPMBPWR	HLTHY#	VIO	N/C	N/C	GND
3	INTA#	N/C	N/C	5V	N/C	GND
2	N/C	5V	N/C	N/C	N/C	GND
1	5V	-12V	N/C	+12V	5V	GND

Table 2-19: J17 Connector Pin Assignment

2.10.14 Hot Swap Micro Switch Connector (J18)

This connector is a 3-pin 0.050" keyed Molex

Pin Number	Signal
1	Switch Input
2	GND
3	5V

Table 2-20: J18 Pin Assignments

2.10.15 Speaker Connector (J19)

This header is an industry standard 2-pin 0.1" keyed Molex

Pin Number	Signal
1	Fused 5V
2	Speaker

Table 2-21: J19 Pin Assignment

2.10.16 IDE/Floppy Mezzanine Connector (J20)

The IDE/Floppy mezzanine connector uses a male 2x25 header with 2mm spacing. The mezzanine connector supports various storage devices such as hard drives, floppy drives, and Compact Flash. The primary intent of the mezzanine board is to add a storage device without exceeding the single slot board height permissible by ComapcPCI.

Pin	Signal	Pin	Signal
1	5V	2	GND
3	RESET#	4	HSD8
5	HSD7	6	HSD9
7	HSD6	8	HSD10
9	HSD5	10	HSD11
11	HSD4	12	GND
13	HSD3	14	HSD12
15	HSD2	16	HSD13
17	HSD1	18	HSD14
19	HSD0	20	HSD15
21	HSDRQ	22	HSIOW#
23	HSIOR#	24	HSIOCHRDY
25	GND	26	5V
27	HSDAK#	28	HSIRQ14
29	HSADDR1	30	HSADDR0
31	HSADDR2	32	HSCS1#
33	HSCS0#	34	FINDX#
35	FDS0#	36	FDCHG#
37	GND	38	FDR1#
39	FMTR0#	40	FDIR#
41	FDNSL#	42	FSTEP#
43	FWDAT#	44	FWGAT#
45	FTRK0#	46	FWP#
47	FRDAT#	48	FHDSL#
49	N/C	50	N/C

Table 2-22: J20 Pin Assignments

2.11 THERMAL CONSIDERATIONS

The 2801 operating temperature is limited by the processor. The maximum operating temperature is dependant on the processors maximum case temperature (Tc) and the amount of cooling provided by the enclosure and heatsink. The 2801 ships from the factory with a passive heatsink for cooling the processor. The heatsink requires forced air cooling to be effective.

The chart below shows the maximum operating temperature for the processor currently shipping with the 2801. The operating temperature is based upon a static environment with forced air of 100 to 900 linear feet per minute (LFM). It is recommended that the engineer perform a complete system thermal analysis that takes into account the system's thermal properties. As different processors and heatsinks become available, these numbers may change.

Airflow (LFM)	Theta-SA (deg C/W)	Max Ambient (deg C), 800MHz PIII
100	7.7	35
200	3.9	67
300	2.8	76
400	2.2	81
500	1.9	84
600	1.6	86
700	1.5	87
800	1.4	88
900	1.3	89
Tjmax = 100 deg C, TDP = 8.5W		

Table 2-23: 2801 Operating Temperature

2.12 Jumper Summary

The following table summarizes the 2801 configuration jumpers.

Jumper	Description
W1-W4	10/100 Base-T Ethernet Destination 1-2 = Rear I/O (J5 CompactPIC) 2-3 = Front I/O (J6 Connector)
W5-W8	10/100 Base-T Ethernet Destination 1-2 = Rear I/O (J5 CompactPCI) 2-3 = Front I/O (J8 Connector)
W9	CMOS Battery Backup Erase 1-2 = Battery Back CMOS 2-3 = Clear CMOS
W10	CompactPCI Satellite Operation IN = Disable CompactPCI bridge for Satellite operation OUT = Enable CompactPCI bridge for Normal operation
W11	CompactPCI Reset Control IN = Enables CompactPCI reset signal to reset IBC2801 OUT = Disables CompactPCI reset from resetting IBC2801
W12	IPMI Mezzanine Voltage Selection 1-2 = IPMI Operating Voltage (J1 CompactPCI) 2-3 = 5V (All CompactPCI)

Table 2-24: 2801 Jumper Summary

2.13 Manufactures Website Links

The section provides links to manufactures websites for parts and specifications used on the 2801.

CompactPCI Specification	
CompactPCI Specification http://www.picmg.org 10/100 Ethernet Controller - Intel 82559ER http://developer.lsilogic.com Ultra160 SCSI Controller - LSI 53C1000 http://developer.intel.com AGP Video – Intel 69030 http://developer.intel.com	Super I/O - Standard Microsystems FDC37B787 http://www.smsc.com Hardware Monitor - National Semiconductor LM87 http://www.national.com Watchdog - Dallas Semiconductor DS1819A http://www.dalsemi.com PCI to PCI Bridge - Intel 21555 http://developer.intel.com

3. BIOS Setup Options

3.1 Entering Setup Screen

The BIOS allows the user to configure the 2801 for various hardware and disk drive configurations. To enter the BIOS setup screen push the keyboard DELETE key during initial power-on. A blue screen will appear with several menu items. Use the up and down keyboard keys to select a particular menu item. Hit the ENTER key to enter into the sub-menu for that item.

To change the settings when in a sub-menu, use the “up arrow” and “down arrow” keys to make selections and the “+” and “-“ keys to toggle between the options for a particular selection.

Most of the items in the BIOS setup are configured by the factory and will not require modification.

3.2 Saving to CMOS

After changing the various setup parameters select the SAVE & EXIT SETUP option to write the changes to the non-volatile CMOS memory. If you do not want to save your changes, select the EXIT WITHOUT SAVING option.

4. Specifications

4.1 Compatibility

CompactPCI Compatibility: PICMG 2.0, Version 2.1

4.2 Electrical

Parameter Operating Voltage	**Specification**	
	Minimum	Maximum
VCC = 5V	4.75 VDC	5.25 VDC
VCC = 3.3V	3.0 VDC	3.6 VDC

Parameter **Operating Current**		**Specification**	
		Typical	Maximum
Single PIII, 800MHz 512MB DRAM	VCC = 5V	3.4A	4.3 A
	VCC = 3.3V	2.0 A	2.5 A
Dual PIII 800MHz, 512MB DRAM	VCC = 5V	4.9A	6.1 A
	VCC = 3.3V	2.9 A	3.6 A

4.3 Mechanical

Parameter	Specification
Dimensions, Length x Width	6U (220mm X 233.5 mm)
Dimensions, Height	4HP (one slot)
Weight	17.2 oz.

4.4 Environmental

Parameter	Specification
Operating Temperature, Ta (300 LFM of forced cooling - see Table 2-22 for other air flows)	0 to +76C
Storage Temperature, Ts	-40 to +85C
Non-condensing Relative Humidity	Less than 95% at 40C

Appendix 1 – Glossary of Terms

A1 - Glossary of Terms

B

Backplane: A circuit board that mounts to the card cage and provides the connectors that accept the computer board and the expansion peripheral boards. The primary function of the backplane is to provide a signal path between the various slots of the card cage.

Bi-directional parallel port: An 8-bit or 16-bit port used to interface to printers or other high speed parallel devices.

Bridge: A device that interconnects two independent buses. Examples include the bridge between the host processor bus and the PCI bus, the bridge between the PCI bus and a standard expansion bus (such as ISA), and the bridge between two PCI busses.

Bus: An electrical signal path between the electrical devices. A bus can be parallel where each conductor propagates a single bit of data or a bus can be serial where a software protocol is used to share a single conductor among multiple bits of data.

C

Cache: A relatively small amount of high-speed static RAM used to keep copies of information recently read from system DRAM memory. If the host processor should request any of the information currently in the cache, it will be returned to the processor in shorter time than if it came from the system DRAM.

Card Cage: A metal frame that includes individual slots for housing the computer boards and a backplane for providing the communication path between them.

CompactPCI: CompactPCI is a variation of the PCI standard for use in industrial and embedded applications. CompactPCI is 100% compatible with the PCI standard in terms of electrical, logical, and software functionality. The form factor for the CompactPCI boards is based on the highly standardized IEEE 1101.1 Eurocard packaging. The primary PICMG specifications are listed below.

- PICMG 2.0 CompactPCI
- PICMG 2.1 Hot Swap
- PICMG 2.5 Telephony
- PICMG 2.11 Power Interface
- PICMG 2.9 System Management
- PICMG 2.12 Infrastructure Interface
- PICMG 2.16 Packet Switching Backplane
- PICMG 2.17 Star Fabric

CPCI (CompactPCI): See CompactPCI.

CMOS (Complementary Metal Oxide Semiconductor): A technology of arranging transistors on a semiconductor which uses very low power.

D

Disk access LED: A status Light Emitting Diode that indicates hard disk activity. The disk access LED is typically located on the front panel.

DRAM (Dynamic Random Access Memory): The primary type of memory used by the computer for program execution and data storage. Several types of DRAM have developed over the years. These include EDO DRAM (Extended Data Out DRAM), SDRAM (Synchronous DRAM), RDRAM (RAMbus DRAM), and DDR DRAM (Double Data Rate DRAM). DRAM is volatile, meaning that the data is lost when the power is removed.

Drive bay: Area in the chassis where drives are mounted.

E

Electrostatic discharge (ESD): A sudden uncontrolled movement of accumulated electrical charge from one location to another. Voltage potentials and discharge currents associated with ESD can damage many types of electronic components used in computers. ESD prevention methods should always be employed when servicing computer hardware.

EMI (Electromagnetic Interference): Noise generated by the switching action of the power supply and other system components. Conducted EMI is interference generally conducted into the power line, and is normally controlled with a line filter. Radiated EMI is that portion that radiates into free space, one way to suppress it is by enclosing circuitry in a metal case.

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power.

Expansion card: A peripheral board that plugs into an expansion slot for adding capabilities to the computer.

F

Floppy drive: A device that accepts floppy disks. Floppy disks are useful for transferring small amounts of data into or out off the computer. A floppy disk typically stores 1.44Mbytes of data.

Front panel: The metal panel on the front of the computer that contains operator interface devices such as a power switch, reset switch, status lights, and various connectors.

H

Hard drive: A non-volatile data storage device. Hard drives magnetically store computer data on spinning internal disks.

Hierarchical PCI Buses: When one PCI bus is subordinate to another PCI bus they are arranged in a hierarchical order. A PCI bridge would interconnect the two buses.

Appendix 1 – Glossary of Terms

I

IDE (Integrated Drive Electronics): A standard protocol for communicating with a hard drive, CD-ROM drive, or other storage device.

I/O card: A peripheral card designed to plug into an expansion slot on a computer to add functionality needed by the application.

I/O slot: A slot designed to accept a specific I/O card.

ISA (Industry Standard Architecture): The original bus architecture used to add functionality to the PC. This architecture, which proceeded PCI, was introduced with an 8-bit data width and later expanded to 16-bits.

K

Keyboard connector: The connector through which keyboard signals are interfaced to the computer.

Kilobyte (KB): A measure of data storage exactly equal to 1,024 bytes.

L

LED: A Light Emitting Diode is a special semiconductor device that emits light when a current passes through it. These long lasting, low power, high efficiency devices are typically used as status indicators.

Load Board: A board having specific power load characteristics which are typically used for testing.

P

Parallel Port: A peripheral device that communicates with multiple data lines to a printer or other parallel interface device. The parallel port is usually a 25-pin female DB25 connector.

PCI (Peripheral Component Interconnect): A computer expansion bus developed by Intel and standardized by the PCI Industrial Computers Manufactures Group (PICMG). Primary features of the PCI bus include bus speeds up to 66MHz; data bus widths up to 64-bits; support for bus masters; independent address spaces for memory , I/O, and configuration; and all of this in less than 50 pins.

Port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

Power Good: A logic signal used to indicate that DC output from a PC power supply has stabilized. The power good line switches from 0 to +5 volts within one tenth to one half second after the power supply reaches normal voltage levels. Whenever output voltage is out of normal operating range for any reason, the power good signal goes back to zero.

Power on LED: A status LED generally located on the front panel to indicate that acceptable power is applied to the computer.

Power Supply: Devices that convert Alternating Current (AC) or Direct Current (DC) source power into the lower level DC voltages required by the computer. Voltages generated by a typical power supply include 3.3V, +/-5V, and +/-12V .

Power Switch: The power switch turns main source power on and off. It is usually located on the front panel or the rear panel near the input power cable.

R

RAID (Redundant Arrays of Independent Disks): A storage technology using an array of two or more disks to redundantly store information. If one RAID disk fails, the unit continues to function without loss of data.

RAM (Random Access Memory): See DRAM.

Real Time Clock (RTC): A peripheral device driven by a constant frequency crystal to provide an accurate time base for the computer. A battery is typically used to ensure the real-time clock continues to operate in the absence of primary power.

Rear panel: The metal panel on the rear of the chassis that provides an alternative to connecting cables to the front panel. Connecting cables to the rear panel instead of the front panel enables the computer or peripheral board to be removed without having to first unplug the cables.

Reset Switch: A push button that reboots the computer. All current activities are stopped and any data in memory is lost.

S

SCSI (Small Computer System Interface): A high-speed parallel interface bus designed to offload block data transfers from the host processor.

SDR (Sensor Data Record): A record of data about a sensor. The full description of the contents of these records can be found in the IPMI specification.

SEL (System Event Log): A non-volatile storage area and associated interfaces for storing system platform event information for later retrieval.

Serial Port: A peripheral device that facilitates data communication between the computer and an external device. The serial channel typically includes a transmit data line, a receive data line, and various handshake lines for coordinating the data transfers.

W

Watchdog Timer: A peripheral device that optionally monitors system operation to be sure that the application software is executing as designed. The watchdog timer generates a hardware reset if it is not accessed by the application software within the minimum time interval.

LIMITED WARRANTY

I-Bus warrants this product to be free of defects in material and workmanship for an initial period of one (1) year from date of delivery to the original purchaser from I-Bus.

During this period, I-Bus will, at its option, repair or replace this product at no additional charge to the purchaser, except as set forth in this warranty agreement.

I-Bus will, at its option, repair or replace this product at no additional charge to the purchaser, if the defect is related to the I-Bus manufactured product, such as power supply, backplanes, other chassis components, or CPUs. I-Bus is not liable for any defects in material or workmanship of any peripherals, products or parts which I-Bus does not design or manufacture. However, I-Bus will honor the original manufacturer's warranty for these products.

I-Bus will analyze the defective component and the customer will be charged.

Receipt of damaged goods voids the I-Bus warranty.

Repair parts and replacement products will be furnished on an exchange basis and will be either new or reconditioned. All replacement parts and products shall become the property of I-Bus, if such parts or products are provided under this warranty agreement. In the event a defect is not related to the I-Bus manufactured product, I-Bus shall repair or replace the defective parts at purchaser's cost and deliver the defective parts to the purchaser.

This Limited Warranty shall not apply if the product has been misused, carelessly handled, defaced, modified or altered, or if unauthorized repairs have been attempted by others.

The above warranty is the only warranty authorized by I-Bus and is in lieu of any implied warranties, including implied warranty of merchantability and fitness for a particular purpose.

In no event will I-Bus be liable for any such damage as lost business, lost profits, lost savings, downtime or delay, labor, repair or material cost, injury to person or property or any similar or dissimilar consequential loss or damage incurred by purchaser, even if I-Bus has been advised of the possibility of such losses or damages.

In order to obtain warranty service, the product must be delivered to the I-Bus facility, or to an authorized I-Bus service representative, with all included parts and accessories as originally shipped, along with proof of purchase and a Returned Merchandise Authorization (RMA) number.

The RMA number is obtained, in advance, from I-Bus Customer Service Department and is valid for 30 days. The RMA number must be clearly marked on the exterior of the original shipping container or equivalent. Purchaser will be responsible and liable for any missing or damaged parts. Purchaser agrees to pay shipping charges one way, and to either insure the product or assume the liability for loss or damage during transit. Ship to:

I-Bus (see page 2 for I-Bus address)
ATTENTION: RMA REPAIR DEPT.
RMA ####

Appendix 3 – FCC Information

A3 - FCC Information

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

WARNING: This equipment has been tested and found to comply with the limits for a Class "A" digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This product was FCC verified under test conditions that included the use of shielded I/O cables and connectors between system components. To be in compliance with FCC regulations, the user must use shielded cables and connectors and install them properly.