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Chapter 1 Introduction

Welcome to the I-Bus family of passive backplane CPU boards. This manual contains the information necessary to configure your CPU board to your specific needs.

The Orca™ passive backplane CPU board is IBM PC/AT- compatible utilizing 5V or 3.3V, 486-compatible processors.

This chapter is divided into three sections:

- About this manual

  explains how this manual is laid out and what you can expect to find in it.

- Preparing the board

  describes the procedure for unpacking the Orca CPU board and preparing it for use in your system.

- Features of the board

  provides a brief overview of the major components of the Orca CPU board accompanied by an illustration of the board showing its jumpers, connectors and components. For convenient reference, a fold-out version of this illustration is provided at the back of this manual.

About this manual

The first three chapters of this manual pertain to your specific CPU board. The appendices contain technical reference material, a glossary of terms, a fold-out illustration of the board, and the BIOS setup utility, followed by an index.

- ### Chapter 1 Introduction

  introduces you to this manual and to the Orca CPU board.

- ### Chapter 2 Jumpers and Connectors

  describes the jumpers and connectors on the Orca CPU board. First, each jumper is described. A table shows on which pins to place the jumper for your specific configuration and an illustration of the jumper shows the pin locations. Then, each connector is described. A table shows the pin-out descriptions and an illustration shows the pin locations for each connector.

- ### Chapter 3 Specifications

  provides the component data and environmental characteristics of the Orca CPU board.

- ### Appendix 1 Technical Reference

  provides additional information that can help you configure your CPU board and attach external peripheral devices. These include I/O Maps, I/O Channels, Interrupts and Address Maps and ISA pin assignments.

- ### Appendix 2 Glossary of Terms

  contains definitions of terms used in this manual as well as terms that refer to items discussed.

- ### Appendix 3 Illustration

  provides a convenient fold-out illustration of the Orca CPU board.

- ### Appendix 4 BIOS

  explains the setup utility and how to use it.

- Index

  provides easy access to page numbers of items discussed.

Preparing the board

- Unpacking your CPU board

  The Orca CPU board is shipped in a sealed, anti-static shielded bag.

  - Open the bag at a static-free workstation while observing proper Electrostatic Discharge (ESD) practices.
  - When not installed in a computer chassis, this board must be sealed in an ESD approved shielded bag.
  - This board must be shipped in a sealed ESD approved shielded bag and protected with anti-static packaging material (e.g. bubble wrap).
  - I-Bus reserves the right to refuse warranty service on units not properly packaged to protect against ESD damage.

CAUTION!

Components on this board are sensitive to damage from Electrostatic Discharge (ESD). Handling of this board should ONLY be done by a properly trained technician in an approved ESD work area!

Packaged with the Orca CPU board are:

- an *Orca Passive Backplane CPU Board User Manual*
- Optional memory
- a Keyboard adapter cable
- Optional cables

If any of the items have been damaged in shipping, notify the transit company and initiate an insurance claim. If any items are missing, contact I-Bus. Refer to the *Limited Warranty* in the back of this manual for further instructions.

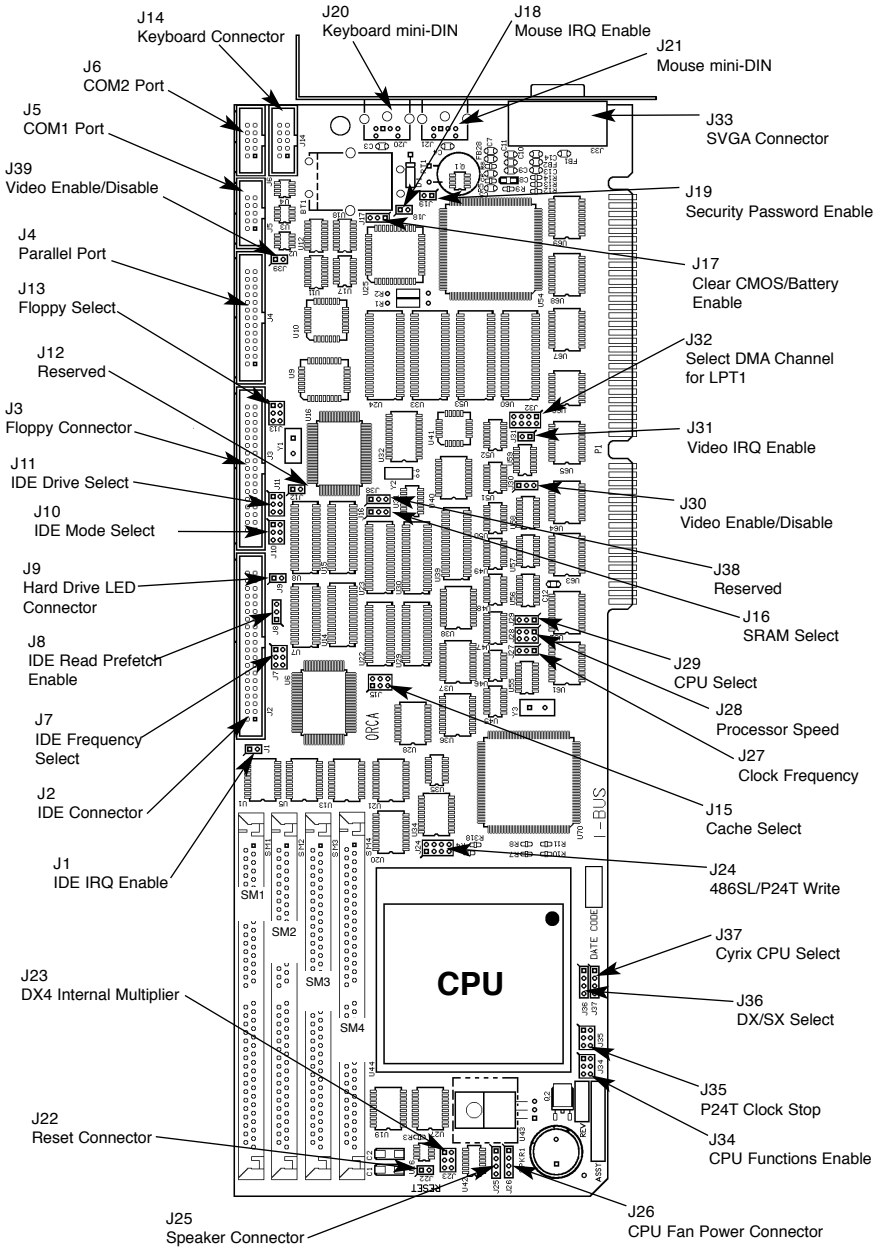


Figure 1-1: Orca CPU Board Jumpers, Connectors, and Components

Features

The key features of the Orca CPU board are:

- **Supports 486SX through P24T Pentium™ Upgrade Central Processing Units (CPUs)**
- **256K or 512K cache memory**
- **Supports up to 128MB DRAM**
- **Two high speed serial ports (16550 type UARTS)**
- **One bidirectional parallel port with DMA access**
- **Floppy disk interface supporting up to two 2.88MB disk drives**
- **Local bus Enhanced Integrated Drive Electronics (EIDE) hard disk interface**
- **Real-time clock with on-board battery backup**
- **On-board battery with 2 year life expectancy**
- **Keyboard, mouse, speaker, and reset ports**
- **Watchdog timer, two-level**
- **Local bus SVGA video with up to 2MB display memory**

The following are detailed descriptions of the above features:

- ### 486SX through P24T Pentium Upgrade CPU

  The Orca supports the 486SX @ 25MHz and 33MHz, 486DX @ 33MHz and 50MHz, 486DX2 @ 50MHz and 66MHz, DX4 @ 100MHz, and the P24T Pentium Upgrade CPUs.

- ### Cache

  The Orca is equipped with 256K write back cache.

• DRAM

The Orca CPU board supports up to 128MB of 72-pin DRAM SIMMs located in four sockets. Sockets are labeled SM1 through SM4.

Total	SM1	SM2	SM3	SM4
4MB	--------	--------	--------	4MB (1MB x 36)
8MB	--------	--------	--------	8MB (2MB x 36)
16MB	--------	--------	--------	16MB (4MB x 36)
32MB	--------	--------	--------	32MB (8MB x 36)
8MB	--------	--------	4MB (1MB x 36)	4MB (1MB x 36)
16MB	--------	--------	8MB (2MB x 36)	8MB (2MB x 36)
32MB	--------	--------	16MB (4MB x 36)	16MB (4MB x 36)
64MB	--------	--------	32MB (8MB x 36)	32MB (8MB x 36)
128MB	--------	--------	64MB (16MB x 36)	64MB (16MB x 36)
16MB	4MB (1MB x 36)	4MB (1MB x 36)	4MB (1MB x 36)	4MB (1MB x 36)
24MB	4MB (1MB x 36)	4MB (1MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)
40MB	4MB (1MB x 36)	4MB (1MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
72MB	4MB (1MB x 36)	4MB (1MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
32MB	8MB (2MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)
48MB	8MB (2MB x 36)	8MB (2MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
80MB	8MB (2MB x 36)	8MB (2MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
64MB	16MB (4MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
96MB	16MB (4MB x 36)	16MB (4MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
128MB	32MB (8MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)

Table 1-1: DRAM Configurations

For other possible configurations, contact I-Bus.

• Multifunction Controller (XIO)

The multifunction controller provides two high speed serial ports, one bidirectional parallel port, and a floppy disk controller.

• IDE Controller

The IDE controller is supported by VESA 32-bit local bus with four-level read prefetch.

• Serial I/O Interface

There are two RS232-compatible serial communication ports with 16550 type UARTS: a primary serial port at J5 and a secondary serial port at J6.

- ## Parallel I/O Interface

  The Orca CPU board provides a parallel I/O interface at J4. While it is conventionally a printer port, it can be reconfigured by software to be a bidirectional parallel port. Contact I-Bus for information.

- ## Floppy Disk Drive Interface

  Any combination of up to two 3.5" and/or 5.25" disk drives or up to two 2.88MB drives can be installed on the Orca CPU board at J3. The interface can also be disabled through the BIOS.

- ## OPTi 82C802G

  The OPTi 82C802G provides the major portion of the system control. Its features include cache interface, buffer controller, memory interface, system and cache controllers. The "G" indicates support for green functions.

- ## Integrated Peripheral Controller (IPC)

  The 82C802G integrates two 8237 DMA controllers, two 8259 interrupt controllers and one 8254 timer/counter.

- ## Programmable Interrupt Controller

  The 82C802G provides 15 user selectable interrupt channels.

- ## Counter/Timer

  The 82C802G provides three independent counter channels. Counter 0 is used as a system timer. Counter 1 is used to generate pulses for DRAM refresh. Counter 2 is a full function counter/timer.

• Direct Memory Access (DMA)

The 82C802G provides seven DMA channels. The first four DMA channels are used for eight-bit DMA transfers. The remaining three channels are used for sixteen-bit DMA transfers. The sixteen-bit DMA channels function identically to the eight-bit DMA channels except that bit 0 of the address and the length fields are assumed to be zero. (All transfers must begin on an even address boundary and the length must be an even number of bytes.) The sixteen-bit DMA channels transfer up to 128KB while the eight-bit DMA channels transfer up to 64KB.

• IDE Hard Disk Interface

The Orca CPU board provides a Local Bus Enhanced Integrated Drive Electronics (EIDE) interface for up to two IDE hard disk drives through the header at J2. J2 accepts a forty-pin IDE connector.

• Keyboard Interface

The Orca CPU board uses the 8042 keyboard controller. A six-pin mini-DIN connector is provided at J20. A ten-pin header is also provided at J14. A keyboard adapter cable is available for keyboards with a five-pin DIN connector. Contact I-Bus for ordering information.

• Real-time Clock/Calendar

The Orca CPU board has a real-time clock/calendar backed by an on-board battery. It has 114 bytes of CMOS RAM included with the clock. The battery has a two year life expectancy and is field replaceable.

• Reset

An external reset can be attached to the Orca CPU board through the connector at J22.

• Speaker

The Orca CPU board provides an on-board speaker and the capability of adding an external speaker at connector J25.

- ## EPROM

  The 27C010 EPROM contains the BIOS for the system. The system BIOS is mapped from F0000h to FFFFFh.

- ## Bus Drivers

  The Orca CPU board uses buffered bus drivers which are capable of driving nineteen additional expansion cards.

- ## Watchdog Timer

  To operate the watchdog timer on the Orca CPU board, several programming steps are required. After booting the system, perform a byte write to port 160H to reset the watchdog (data value is unimportant). Set the divisor for the RTC square wave output by performing the following steps:

  1. Write a 0AH to port 70H to access port A of the RTC.
  2. Read port 71H to retrieve value.
  3. Logically OR the value read with 0FH.
  4. Write a 0AH to port 70H to access port A of the RTC.
  5. Write the modified value to port 71H.

  Enable the square wave output by executing the following steps:

  1. Write a 0BH to port 70H to access port B of the RTC.
  2. Read port 71H to retrieve value.
  3. Logically OR the value read with 08H.
  4. Write a 0BH to port 70H to access port B of the RTC.
  5. Write the modified value to port 71H.

  The watchdog timer is now running. To reset the watchdog timer, perform a byte write to port 160H. The watchdog timer will time out if no write to port 160H is executed within 16 seconds. At this point, interrupt 11 is asserted. If another 16 seconds passes without a write to port 160H the board is reset.

To disable watchdog timer operation:

1. Write a 0BH to port 70H to access port B of the RTC.
2. Read port 71H to retrieve value.
3. Logically AND the value read with F7H.
4. Write a 0BH to port 70H to access port B of the RTC.
5. Write the modified value to port 71H.

• Local Bus Video

The Orca is equipped with on-board local bus SVGA with up to 2MB video RAM. It incorporates the Cirrus Logic CL-GD5434, and runs at up to 41 million WINMARKS (WINBENCH 3.1) when using a DX4-100 CPU with 2MB display memory. This provides a dramatic improvement in performance over ISA video cards.

- Configurable resolutions up to 1280 x 1024 (256 colors non-interlaced)
- 32-bit wide DRAM interface with 1MB; 64-bit wide DRAM interface with 2MB
- Up to 2MB display memory
- 16.8 million color capability (640 x 480, 800 x 600)
- Backward compatible with VGA, EGA, CGA, MDA
- 15, 16 or 24-bit True Color
- Refresh rates up to 72Hz non-interlaced
- Hardware bit BLT for Microsoft Windows™
- Independent video and DRAM timing

Chapter 2 Jumpers and Connectors

This chapter describes the jumpers and connectors on the Orca CPU board. Jumpers and connectors are identified by the label shown beside them on the board (e.g. J36), followed by the description (e.g. DX/SX Selection). A table shows the jumper settings or connector pin-outs for each jumper and connector. Illustrations of jumpers and connectors are shown from the component side of the board. Pin 1 is identified by the black pin.

All of the jumpers and connectors are shown on the illustration on page 1-4, Figure 1-1, Orca CPU Board Jumpers, Connectors and Components and on the fold-out illustration on page A3-1.

Pin 1 can be identified on the solder side of the board by the square pad in a connector or jumper.

For clarity, in this manual jumpers are divided into two types: CPU Jumpers and Board Jumpers.

- CPU Jumpers, listed in Table 2-1, pertain to settings for the CPU installed on your CPU board.
- Board Jumpers, listed in Table 2-10, pertain to functions of the CPU board and its peripherals.

CAUTION!

Components on this board are sensitive to damage from Electrostatic Discharge (ESD). Handling of this board should ONLY be done by a properly trained technician in an approved ESD work area!

CPU Jumpers

The following jumpers are factory-set for the CPU installed on your CPU board. If you upgrade to another CPU or reconfigure your system, you may need to reset some of the jumpers.

Jumper	Description	No. of Pins
J23	DX4 Internal Multiplier	6
J24	486SL/P24T Write	8
J27	Clock Frequency	3
J29	CPU Select	3
J34	CPU Functions Enable	6
J35	P24T/Clock Stop	6
J36	DX/SX Select	4
J37	Cyrix CPU Select	4

Table 2-1: CPU Jumpers

• J23, DX4 Internal Multiplier

J23 contains a jumper setting if a Cyrix CPU is present. Otherwise, the jumper settings pertain to the internal multiplier of the DX4.

Position	Function
3&4	Cyrix CPU
1&3	DX4 / 2.5X
3&5	DX4 / 2X
None	DX4 / 3X

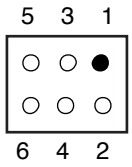


Table 2-2: J23, DX4 Internal Multiplier

• J24, 486SL / P24T Write

Two jumpers must be placed on J24 if your CPU board contains a 486SL CPU (with power management feature). Or, if you have a P24T CPU installed, you can select burst writes, write-back, or write-through cache. Removing the jumper from pins 7 and 8 enables the write-through cache for a P24T CPU.

Position	Function
1&2, 3&4	486SL CPU
5&6	Enable P24T Burst Writes
7&8	Enable P24T Write-Back
No Jumpers	Enable P24T Write-Through

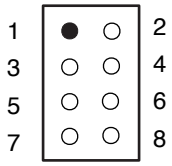


Table 2-3: J24, 486SL / P24T Write

• J27, Clock Frequency

J27 contains jumper settings for the slow clock frequency at 8MHz, or 16MHz for the DX4 CPU.

Position	Function
1&2	8MHz
2&3	16MHz (DX4)

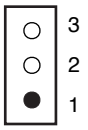


Table 2-4: J27, Clock Frequency

• J29, CPU Select

Jumpers must be set on J29 if an Intel/AMD or Cyrix CPU is present.

Position	Function
1&2	Intel/AMD CPU
2&3	Cyrix CPU

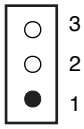


Table 2-5: J29, CPU Select

• J34, CPU Functions Enable

J34 contains a jumper setting to activate the warm reset for a Cyrix CPU. It also contains a setting if a 486SL CPU (with power management feature) is present. Two settings enable the write-back and write-through cache for the P24D CPU with special write-back cache.

Position	Function
4&6	Activate Cyrix CPU
2&4	486SL CPU
3&5	Enable P24D write-back cache
1&3	Enable P24D write-through cache

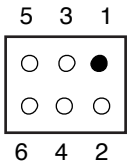


Table 2-6: J34, CPU Functions Enable

• J35, P24T / Clock Stop

J35 contains a jumper setting if a P24T CPU is present. Jumpers are also installed on J35 to select bit 0 or bit 1 of the green port to stop the clock.

Position	Function
1&3	CPUís other than P24T
3&5	P24T
2&4	Bit 0 to stop clock
4&6	Bit 1 to stop clock

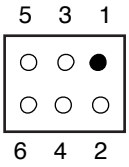


Table 2-7: J35, P24T / Clock Stop

• J36, DX / SX Select

Set jumpers on J36 for 486DX or 486SX operation.

Position	Function
1&2, 3&4	486DX Operation
2&3	486SX Operation

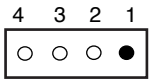


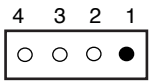
Table 2-8: J36, DX / SX Select

- J37, Cyrix CPU Select

Set jumpers on J37 if your CPU board contains a Cyrix CPU.

Position	Function
1&2, 3&4	Cyrix CPU
OFF	CPU Other than Cyrix

Table 2-9: J37, Cyrix CPU Select



Board Jumpers

The following jumpers control functions of the CPU board and its peripherals.

Jumper	Description	No. of Pins
J1	IDE IRQ Enable	2
J7	IDE Frequency Select	6
J8	IDE Read Prefetch Enable	3
J10	IDE Mode Select	6
J11	IDE Drive Select	6
J12	Reserved	2
J13	Floppy Select	6
J15	Cache Select	6
J16	SRAM Select	3
J17	Clear CMOS / Battery Enable	3
J18	Mouse IRQ Enable	2
J19	Security Password Enable	2
J28	Processor Speed	6
J30	Video Enable/Disable	3
J31	Video IRQ Enable	2
J32	DMA Channel for LPT1	8
J39	Video Enable/Disable	2

Table 2-10: Board Jumpers

• J1, IDE IRQ Enable

Placing a jumper on J1 enables IRQ14 for the IDE. If no jumper is placed on J1, IRQ14 is available for other use.

Position	Function
1&2	Enable IRQ14
OFF	IRQ14 Available

• J7, IDE Frequency Select

This jumper setting must match the frequency of the CPU installed on your CPU board.

Position	Function
4&6, 3&5	50MHz
3&5, 2&4	40MHz
1&3, 4&6	33MHz
1&3, 2&4	25MHz

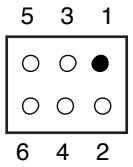


Table 2-12: J7, IDE Frequency Select

• J8, IDE Read Prefetch Enable

Read prefetch allows the controller to access data off the disk in anticipation of its use.

Note: If WindowsNT™ is being used, jumpers ***must be placed on pins 2 and 3*** for proper operation.

Position	Function
1&2	Enable IDE Read Prefetch
2&3	Disable IDE Read Prefetch

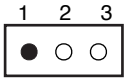


Table 2-13: J8, IDE Read Prefetch Enable

• J10, IDE Mode Select

Select the appropriate disk drive cycle time by placing jumpers on the designated pins.

Position	Function
3 & 5, 4 & 6	> 480ns
1 & 3, 4 & 6	> 383ns
3 & 5, 2 & 4	> 240ns
1 & 3, 2 & 4	> 180ns

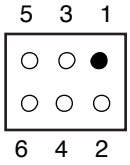


Table 2-14: J10, IDE Mode Select

- ## J11, IDE Drive Select

Select the address for the IDE port. Either one or the other must be installed unless it is disabled.

Position	Function
1&3	Primary IDE
3&5	Secondary IDE
2&4	Enable IDE port
4&6	Disable IDE port

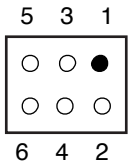


Table 2-15: J11, IDE Drive Select

- ## J12, Reserved - no jumper

- ## J13, Floppy Select

Select the density of the floppy disk drive enabled in the BIOS.

Position	Function
1&2	1.44MB
3&4, 5&6	2.88MB

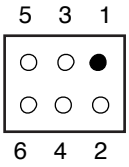


Table 2-16: J13, Floppy Select

- ## J15, Cache Select

Place the jumper on the designated pins for the amount of cache on your CPU board.

Position	Function
no jumpers	64K
5&6	128K
3&4, 5&6	256K
1&2,3&4,5&6	512K

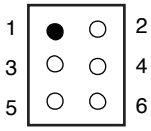


Table 2-17: J15, Cache Select

- ## J16, SRAM Select

J16 contains jumper settings for single bank SRAMs or double bank SRAMs in the cache.

Position	Function
1&2	Single Bank (4)
2&3	Double Bank (8)

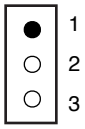


Table 2-18: J16, SRAM Select

- ## J17, CMOS Clear / Battery Enable

J17 contains jumper settings for clearing the system information stored in CMOS and enabling the on-board battery.

Position	Function
1&2	Clear CMOS
2&3	Enable Battery

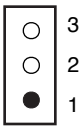


Table 2-19: J17, CMOS Clear / Battery Enable

- ## J18, Mouse IRQ Enable

Placing a jumper on J18 enables IRQ12 for the mouse. If no jumper is placed on J18, the mouse is disabled and IRQ12 is available for other use.

Position	Function
1 & 2	IRQ12 Enabled
OFF	IRQ12 Available

Table 2-20: J18, Mouse IRQ Enable

• J19, Security Password Enable

Installing a jumper on pins 1 and 2 of J19 enables the security password option in the BIOS Setup Utility. With this jumper installed, the password selection is available in BIOS.

Position	Function
1 & 2	Password Enabled
OFF	Password Disabled

Table 2-21: J19, Security Password Enable

• J28, Processor Speed

Select the clock speed of your CPU.

Position	Function
5&6	25MHz
1&2, 5&6	33MHz
3&4, 5&6	40MHz
1&2,3&4,5&6	50MHz

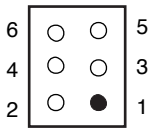


Table 2-22: J28, Processor Speed

• J30, Video Enable/Disable

Installing a jumper on pins 2 and 3 enables the on-board video controller. To disable the on-board video controller, install the jumper on pins 1 and 2. This video selection (video enabled or disabled) ***must be the same as*** jumper J39.

Position	Function
1 & 2	Video Disabled
2 & 3	Video Enabled

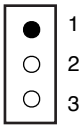


Table 2-23: J30, Video Enable/Disable

- ## J31, Video IRQ Enable

Placing a jumper on J31 enables IRQ9 for video. If no jumper is placed on J31, IRQ9 is available for other use.

Position	Function
1 & 2	IRQ9 Enabled
OFF	IRQ9 Available

Table 2-24: J31, Video IRQ Enable

- ## J32, DMA Channel for LPT1

Using DMA Channels enables high speed transfers from memory to the parallel port. You can select DMA Channels 1 or 3 to be used for the parallel port.

Position	Function
1&2, 7&8	DMA Channel 3
3&4, 5&6	DMA Channel 1

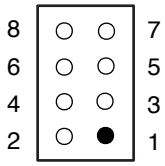


Table 2-25: J32, DMA Channel for LPT1

- ## J39, Video Enable/Disable

Installing a jumper on pins 1 and 2 enables the on-board video controller. To disable the on-board video controller, remove the jumper. This video selection (video enabled or disabled) ***must be the same as*** jumper J30.

Position	Function
1 & 2	Video Enabled
OFF	Video Disabled

Table 2-26: J39, Video Enable/Disable

Connectors

The following connectors can be located in Figure 1-1: ORCA CPU Board Jumpers, Connectors and Components on page 1-4 and on the fold-out illustration at the back of this manual.

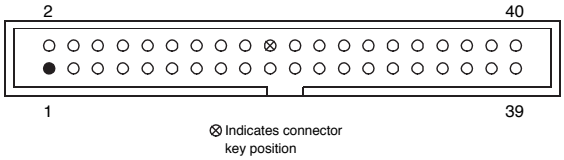
Jumper	Description	No. of Pins
J2	IDE Connector	40
J3	Floppy Connector	34
J4	Parallel Port	26
J5	COM1 Port	10
J6	COM2 Port	10
J9	Hard Drive LED Connector	2
J14	Keyboard Connector - 10 pin	10
J20	Keyboard mini-DIN	6
J21	Mouse mini-DIN	6
J22	Reset Connector	2
J25	Speaker Connector	4
J26	CPU Fan Power Connector	4
J33	SVGA Connector	15

Table 2-27: Connectors

- J2, IDE Connector

Pin #	Name	Pin #	Name
1	$\overline{\text{RST}}$	21	N/C
2	GND	22	GND
3	D7	23	IOW
4	D8	24	GND
5	D6	25	IOR
6	D9	26	GND
7	D5	27	N/C
8	D10	28	BALE
9	D4	29	N/C
10	D11	30	GND
11	D3	31	IRQ14
12	D12	32	IO16
13	D2	33	SAI
14	D13	34	N/C
15	D1	35	SA0
16	D14	36	SA2
17	D0	37	CS0
18	D15	38	CS1
19	GND	39	HDIND
20	Key	40	N/C

Table 2-28: J2, IDE Connector

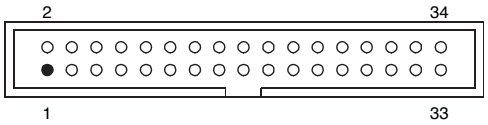


- J3, Floppy Connector

Pin #	Name
2	RMP/LC
4	N/C
6	ID0
8	$\overline{\text{INDEX}}$
10	$\overline{\text{MTRO}}$
12	$\overline{\text{DRV1}}$
14	$\overline{\text{DRV0}}$
16	$\overline{\text{MTR1}}$
18	DIR
20	$\overline{\text{STEP}}$
22	$\overline{\text{WDATA}}$
24	$\overline{\text{WGATE}}$
26	$\overline{\text{TRK0}}$
28	$\overline{\text{WPRT}}$
29	ID0
30	$\overline{\text{RDATA}}$
32	HDSEL
33	ID1
34	DSKCHG
*	GND

Table 2-29: J3, Floppy Connector

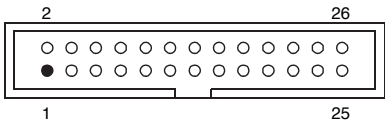
* The remainder of the odd numbered pins are GND.



- J4, Parallel Port

Pin #	Name	Pin #	Name
1	$\overline{\text{Strobe}}$	2	AutoFeed
3	+ Data bit 0	4	Error
5	+ Data bit 1	6	Init
7	+ Data bit 2	8	SLCT IN
9	+ Data bit 3	10	GND
11	+ Data bit 4	12	GND
13	+ Data bit 5	14	GND
15	+ Data bit 6	16	GND
17	+ Data bit 7	18	GND
19	ACK	20	GND
21	Busy	22	GND
23	Paper Empty	24	GND
25	GND	26	N/C

Table 2-30: J4, Parallel Port

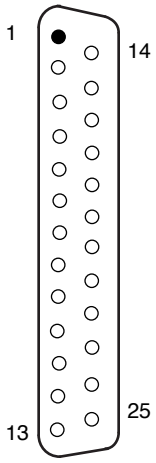


• DB25 Connector

The optional parallel port cable connects to J4 on the CPU board and contains a DB25 connector which attaches to the I/O panel on the back of the chassis.

Pin#	Name
1	-Strobe
2	+Data bit 0
3	+Data bit 1
4	+Data bit 2
5	+Data bit 3
6	+Data bit 4
7	+Data bit 5
8	+Data bit 6
9	+Data bit 7
10	ACK1
11	Busy
12	Paper Empty
13	SLCT
14	AutoFeed
15	Error
16	Init
17	SLCT IN
18-25	GND

Table 2-31: DB25 Connector



- J5, COM1 Port

The primary serial port is a ten-pin header located at J5. You can terminate the primary serial port in a DB9 connector by obtaining the optional serial port cable from I-Bus. A wire list is also provided on page 2-19 if you want to make your own cable.

Another optional cable from I-Bus contains a retaining bracket with a DB9 and a DB25 connector terminating in a ten-pin and twenty-six-pin header, respectively.

Pin #	Name
1	$\overline{\text{DCD}}$
2	$\overline{\text{DSR}}$
3	RXD
4	$\overline{\text{RTS}}$
5	TXD
6	$\overline{\text{CTS}}$
7	$\overline{\text{DTR}}$
8	$\overline{\text{RI}}$
9	GND
10	N/C

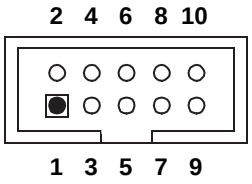


Table 2-32: J5, COM1 Port

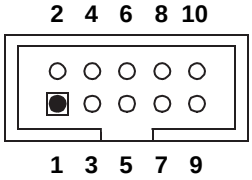
• J6, COM2 Port

The secondary serial port is a ten-pin header located at J6. You can terminate the secondary serial port in a DB9 connector by obtaining the optional serial port cable from I-Bus. A wire list is also provided on page 2-19 if you want to make your own cable.

Another optional cable from I-Bus contains a retaining bracket with a DB9 and a DB25 connector terminating in a ten-pin and twenty-six-pin header, respectively.

Pin #	Name
1	$\overline{\text{DCD}}$
2	$\overline{\text{DSR}}$
3	RXD
4	$\overline{\text{RTS}}$
5	TXD
6	$\overline{\text{CTS}}$
7	$\overline{\text{DTR}}$
8	$\overline{\text{RI}}$
9	GND
10	N/C

Table 2-33: J6, COM2 Port



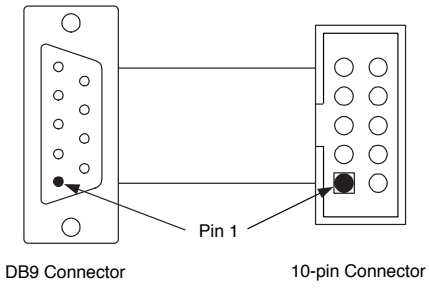
• Serial Port Cable Wire List

The following wire list is provided for users who want to make a cable that connects to a serial port connector (J5 or J6) and terminates with either a DB9 or DB25 (RS232) connector. For the locations of J5 and J6, refer to Figure 1-1, ORCA CPU Board Jumpers, Connectors and Components on page 1-4.

Signal Name	Connector		
	Onboard 10 Pin Connector (J5 or J6)	25 Pin	9 Pin
$\overline{\text{DCD}}$	1	8	1
$\overline{\text{DSR}}$	2	6	6
RXD	3	3	2
$\overline{\text{RTS}}$	4	4	7
TXD	5	2	3
$\overline{\text{CTS}}$	6	5	8
$\overline{\text{DTR}}$	7	20	4
$\overline{\text{RI}}$	8	22	9
GND	9	2	5
N/C	10	N/C	N/C

Table 2-34: Serial Port Cable Wire List

The following cable assembly shows the Pin 1 locations for the DB9 and ten-pin connectors. Serial port cables with DB9 and DB25 connectors are also available through I-Bus.



- J9, Hard Drive LED Connector

An LED can be connected at J9 to display hard drive activity.

Pin#	Name
2	Anode
1	Cathode

Table 2-35: J9, Hard Drive LED Connector

- J14, Keyboard Connector - 10-pin

Pin #	Name
1	CLOCK
2	GND
3	DATA
4	N/C
5	N/C
6	N/C
7	+5 V
8	Key
9	N/C
10	GND

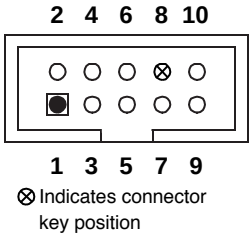
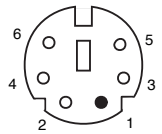


Table 2-36: J14, Keyboard Connector - 10-

• J20, Keyboard mini-DIN

J20 is a six-pin mini-DIN keyboard connector located on the retaining bracket. You can also use a standard PC/AT-compatible keyboard fitted with the keyboard adapter cable furnished with your CPU board. Or, you can use the ten-pin keyboard header at J14.

Pin #	Name
1	DATA
2	N/C
3	GND
4	+5 V
5	CLOCK
6	N/C



View from end of board

Table 2-37: J20, Keyboard mini-DIN

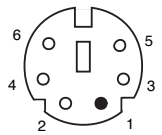
CAUTION!

The mouse and keyboard mini-DIN connectors are identical. Make sure the correct accessory is plugged into it's proper connector.

• J21, Mouse mini-DIN

J21 is a six-pin mini-DIN mouse connector located on the retaining bracket.

Pin #	Name
1	DATA
2	N/C
3	GND
4	+5 V
5	CLOCK
6	N/C



View from end of board

Table 2-38: J21, Mouse mini-DIN

• J22, Reset Connector

An external reset cable can be attached to the ORCA at J22.

Pin#	Name
2	Reset
1	GND

Table 2-39: J22, Reset Connector

• J25, Speaker Connector

Placing a jumper on pins 1 and 2 of J6 enables the on-board speaker. You can attach an external speaker to the ORCA by connecting a four position connector to J25.

Pin#	Name
1	External Speaker
2	Internal Speaker
3	VCC
4	VCC

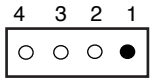


Table 2-40: J25, Speaker Connector

• J26, CPU Fan Power Connector

You can connect a CPU fan by connecting a four-position connector to J26.

Pin#	Name
1	+12V
2	N/C
3	N/C
4	GND

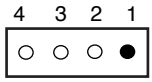


Table 2-41: J26, CPU Fan Power Connector

• J33, SVGA Connector

J33 is a 15-pin connector located on the retaining bracket and connecting the SVGA with the system monitor.

Pin#	Name
1	Red Drive
2	Green Drive
3	Blue Drive
4	N/C
5	GND
6	GND
7	GND
8	GND
9	N/C
10	GND
11	N/C
12	N/C
13	HORIZ SYNC
14	VERT SYNC
15	N/C

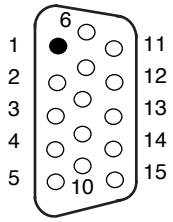


Table 2-42: J33, SVGA Connector

Chapter 3 Specifications

System Components

CPU:	486SX/33 & 100, 486DX/50 & 66, DX4, P24T
Form Factor:	Standard full length AT
Interrupts:	15 levels available
Power Requirements:	Input Power with DX4-100 CPU and 4MB DRAM +5V @ 4.6A +12V @ 50mA -12V @ 50mA
Cache:	256K or 512K standard write-back cache
Dynamic RAM:	2MB to 128MB on-board 36-bit DRAM SIMM
System ROM:	Contains system & video BIOS
Clock/Calendar:	Real-time clock backed by an on-board lithium battery
External Connections:	IDE & floppy (shrouded headers) Bidirectional parallel port (shrouded header) Serial port 1 (shrouded header) Serial port 2 (shrouded header) Keyboard (mini-DIN on retaining bracket) PS/2 Mouse (mini-DIN on retaining bracket) Keyboard (Ten-pin header) Speaker (header) Reset (header) Hard Drive LED (header) SVGA (15-pin connector on retaining bracket)
Watchdog Timer:	Two-stage, software programmable

Environmental Specifications

SVGA Connector: Configurable resolutions up to 1280 x 1024 (256 colors non-interlaced)
32-bit wide DRAM interface with 1MB display memory
64-bit wide DRAM interface with 2MB display memory
Up to 2MB display memory
16.8 million color capability (640 x 480, 800 x 600)
Backward compatible with VGA, EGA, CGA, MDA
15, 16 or 24-bit True Color
Refresh rates up to 72Hz non-interlaced
Hardware bit BLT for Microsoft Windows™
Independent video and DRAM timing

Environmental Specifications

Environmental	Operating	Non-operating
Temperature	0∞ to +55∞C	-40∞ to +65∞C
Humidity	5 to 95% @ 40∞C non-condensing	5 to 95% @ 40∞C non-condensing
Shock	2.5 g @ 10 ms	10 g @ 10 ms
Vibration	0.25 g @ 5-100 Hz	5 g @ 5-100 Hz

Table 3-1: Environmental Specifications

Agency

All I-Bus CPU boards meet UL 1950, CSA 22.2 No. 950, TUV and IEC 950, and FCC Part 15 Class A in I-Bus enclosures. Customer requested FCC, VDE and CISPR Class B certification available.

The BIOS Setup Utility allows you to configure your CPU (Central Processing Unit) board to your system. The BIOS, or Basic Input/Output System, is the on-board firmware that communicates with the display, keyboard, printers and other peripheral devices.

Starting and Exiting the BIOS Setup

When you turn on your computer, a test is conducted called the Power On Self Test, or POST. During this test the system checks for certain hardware configurations and compares them to the BIOS Setup Utility. If, at boot, the system status does not match the system configuration stored in CMOS, you will be prompted to start the BIOS Setup Utility. This occurs if the "Initialization Errors Halt" prompt is set to "Active" in the Boot Sequence setup screen. If set to "Inactive," the system continues to boot.

To Start the BIOS Setup:

- During a cold boot, press <Esc> while the memory size is scrolling on the screen.
- While in DOS, press <Ctrl> + <Alt> + <Esc>. (When you exit the BIOS, the system automatically reboots).

To Exit the BIOS Setup and boot the computer:

- While in a utility screen, move the cursor to the menu line at the top of any screen and press <F10>. All configuration changes edited in the various screens are recorded in CMOS memory at this time. If, however, you turn off the power or press the front panel reset button without pressing <F10>, the changes you made in the BIOS will not be saved and the original configuration will remain unchanged.

The screens presented in this manual reflect the same format as your screens but **they do not contain parameters**.

• All BIOS screens contain:

- **menu line** at the top of the screen containing names of the utilities available from that screen.
- **body** consisting of the **entry fields** containing the utility's parameters.
- **bottom line** indicating the keystrokes that you can use to manipulate the cursor in that screen.

• Manipulating the screens

A reverse video cursor is always present, either on the menu line or in the body.

- Use the <Right Arrow> and <Left Arrow> keys to move the cursor across the menu line, highlighting the name of the current utility.
- When a utility's name is highlighted in the menu line, the entry fields of that utility are displayed in the body. Press the <Down Arrow> key to move the cursor into the first entry field. You can move the cursor through the entry fields using the <Down Arrow> key.
- To change an entry field, press <Enter>, then follow the instructions in the bottom line. The instructions change depending on the current field.
- You can scroll through the available choices for that field by pressing the <Spacebar> or the "+" and "-" keys in all adjustable fields. A few fields require alphanumeric entry.
- When all changes have been made to the entry fields, press <Esc> to return the cursor to the menu line. The bottom line changes back to its previous condition.
- When the cursor is in the menu line, you can press <F10> to save your changes and reboot the computer.

- ## Keystrokes

  The following keys are available while the cursor is on the menu line:

Keystroke	Movement
Right, Left Arrow	right and left movement
Space, BackSpace	right and left movement
Tab, Shift-Tab	right and left movement
Home, End	leftmost and rightmost entry
DownArrow, Enter, PgDn	move down into edit window
F10	record and exit Setup

The following keys are generally available within the body:

Keystroke	Movement
Arrows	up, down, left, right
Space, BackSpace	scroll choices in field
Plus, Minus	scroll choices in field
AlphaNumeric	letters and numbers
Enter, (Esc)	begin/end (abort) mode or A/N entry
Esc, PgUp	exit current window, go back to menu

Your System's Parameters

Once you have set your system's parameters, record the settings below. If for any reason you should lose the parameter settings on your system (e.g. the CMOS is reset), you will then be able to easily re-enter them.

Summary

CPU Type _____
CPU Rev _____
CPU MHz _____
PLL Ratio _____
CPU Code Cache _____
CPU Data Cache _____
External Cache _____
Memory - Base _____
Memory - System _____
Memory - Extended _____
Memory - Total _____
Chipset _____
BIOS ID _____
BIOS Date _____

Floppy 0 _____
Floppy 1 _____
Floppy 2 _____
Floppy 3 _____
Fixed 80 _____
Fixed 81 _____
Keyboard _____
NumLock _____
PS2-Mouse _____
Video-Primary _____
Video-Secondary _____

Energy

IDE Drive Timer _____
System Activity _____
Event Monitoring _____
Idle Video State _____

Clock

Display Format _____
Time _____
Date _____
Daylight Savings _____

Keyboard

NumLock State at Bootup _____

Keyboard Typematic Speed _____

Delay Before Keys Repeat _____

Floppy

Floppy 0 _____

Floppy 1 _____

Step-Rate _____

Floppy 2 _____

Floppy 3 _____

Fixed Disk 80

Size _____

_____

Type _____

Cylinders _____

Heads _____

Precomp _____

Landing _____

Sectors _____

_____

Translate _____

Xfer-Mode _____

Anti-Virus _____

Fixed Disk 81

Size _____

_____

Type _____

Cylinders _____

Heads _____

Precomp _____

Landing _____

Sectors _____

_____

Translate _____

Xfer-Mode _____

Your System's Parameters

VL-Bus IDE

Drive 80 (C:) _____ Selectable Rate _____

Drive 81 (D:) _____ External Jumper _____

VL-Bus (LRDY) _____

Boot Sequence

Operating System _____

Boot Sequence _____

Memory Priming _____

Cold-Boot Delay _____

Initialization Error Halts_____

Ports

COM 1 _____ LPT1 _____

COM 2 _____ LPT 2 _____

COM 3 _____ LPT 3 _____

COM 4 _____ LPT 4 _____

Security

Security _____

Speed

System Speed _____

Cache

486-CPU Cache_____ SRAM Write Cycle _____

External Cache _____ Shadow RAM _____

SRAM Burst Read_____ Cache Size _____

Shadow RAM

F000 System	_____	D000 Adapter	_____
E000 Adapter	_____	CC00 Adapter	_____
DC00 Adapter	_____	C800 Adapter	_____
D800 Adapter	_____	C400 Video	_____
D400 Adapter	_____	C000 Video	_____

Chipset

Memory Timing

Wait States - Read_____ A20-Gate Control_____

Wait States - Write_____

Memory Refresh

Method _____ Period_____

AT-BUS Timing

Wait States_____ I/O Recovery_____

AT-Bus Clock_____

37C665

Primary Serial	_____	Parallel Port	_____
Secondary Serial	_____	Floppy	_____

This section describes each setup screen in the Orca BIOS Setup Utility.

Screens are identified in the menu line as:

- **Summary**
- **Energy**
- **Clock**
- **Keyboard**
- **Floppy**
- **Fixed Disk**
- **VL-Bus IDE**
- **Boot Sequence**
- **Ports**
- **Security**
- **Speed**
- **Cache**
- **Shadow RAM**
- **Chipset**
- **37C665**

In this section each utility is represented by:

- **Screen Illustration**
- **Explanation**
- **Entry Fields**

Screen Illustration

The screens presented in this manual reflect the same format as your screens but **they do not contain parameters**.

Explanation

The Explanation following each screen illustration describes the utility and the available choices.

Entry Fields

Each entry field in the body of the screen is described and all available choices, or parameters, are listed in table form.

- Summary Screen

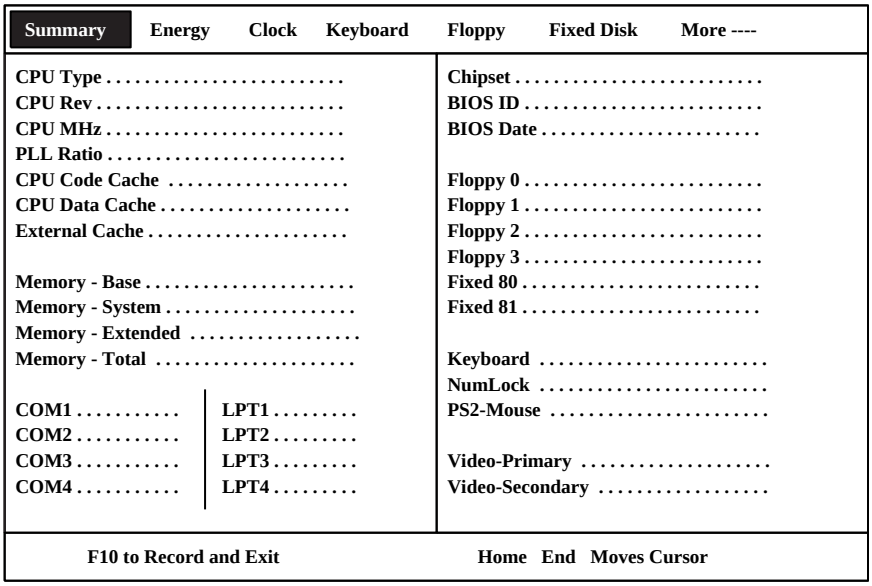


Figure 4-1: Summary Screen

Explanation

The Summary Screen contains information about the hardware on your system. **No user entry is allowed**.

This screen allows you to view system information and indicates when a system component has been properly installed and recognized by the BIOS.

Some of the items on this screen are auto-sensed during the Power On Self Test (POST). Others are determined by selections you make on the following screens.

Items that are auto-sensed are:

CPU Type and MHz	Memory Base and Total
CPU Rev	Video Type
CPU Code Cache	Keyboard Type
CPU Data Cache	Floppy
RAM Cache	Fixed Disk

Review this screen after making configuration changes and prior to exiting the Setup Utility.

Viewing Fields

There is no user entry allowed on this screen.

The parameters displayed are auto-sensed during POST or they are selectable on other screens.

If the BIOS recognizes any serial and parallel ports, their addresses will appear next to the port. If not, "n/a" will appear.

Field	Description	Parameters
CPU Type	Part number of the microprocessor installed in your system (auto-sensed during POST).	1. 486DX4 2. P24T
CPU Rev	Revision level of the CPU (auto-sensed during POST).	1. 0480
CPU MHz	Operating frequency (auto-sensed during POST).	1. 99.7
PLL Ratio	The factor by which the external operating frequency of the system board is multiplied to obtain the internal CPU MHz.	1. 1:1 2. 2:1 3. 3:1
CPU Code Cache	Amount of internal CPU cache allocated for code.	1. 8K
CPU Data Cache	Amount of internal CPU cache allocated for data instructions.	1. 8K
External Cache	How much cache is on the CPU board.	1. 256K 2. 512K
Memory - Base	The amount of Base Memory (at and below the 640K boundary) found to be in working order (auto-sensed during POST).	1. 640K
Memory - System	A portion of memory, typically 384K, reserved for special uses. Some may be allocated to Shadow RAM, and the remainder might automatically be remapped to the Extended Memory pool. This field shows the amount of memory retained for system use.	1. 384K

Table 4-1: Summary Screen Viewing Fields

Field	Description	Parameters
Memory - Extended	The amount of Extended Memory (above the 1MB boundary) found to be in working order.	1. 3 MB 2. 7 MB
Memory - Total	The total amount of memory installed in the system. It is the sum of the three preceding quantities: Base + System + Extended = Total (auto-sensed during POST).	1. 4 MB 2. 8 MB 3. 16 MB
COM1 - 4	Serial ports auto-sensed by the BIOS.	1. n/a 2. Port address(es)
LPT1 - 4	Parallel ports auto-sensed by the BIOS.	1. n/a 2. Port address(es)
Chipset	Permits optional fine tuning of certain chipset parameters.	Opti 802G
BIOS ID	BIOS Type.	OptI9CI
BIOS Date	Date BIOS was built.	mm/dd/yy
Floppy 0 - 3	The floppy drives configured in the system and usually named A or B (auto-sensed during POST).	1. None 2. 5º, 360K 3. 3Ω, 720K 4. 5º, 1.2MB 5. 3Ω, 1.4MB 6. 3Ω, 2.8MB
Fixed 80 - 81	The configured Size and Type for Fixed Disk Drives 80 and 81, usually named C and D, respectively (auto-sensed during POST).	1. None 2. Size [type]
Keyboard	Keyboard type (auto-sensed during POST).	1. PC/AT 2. AT/PS2
NumLock	The NumLock state (auto-sensed during POST). This field is only meaningful for 101 key keyboards. See **Keyboard Screen** description in this Chapter.	1. Off 2. On

Table 4-1: Summary Screen Viewing Fields (continued)

Field	Description	Parameters
PS2-Mouse		1. n/a
Video - Primary	The main video display adapter which will be in use when control is passed to an Operating System at power-up (auto-sensed during POST).	1. None 2. V/EGA - Color 3. Mono
Video - Secondary	Indicates the presence of a second video adapter. It will remain idle until activated by specialized software.	1. n/a 2. Mono

Table 4-1: Summary Screen Viewing Fields (continued)

- Energy Screen

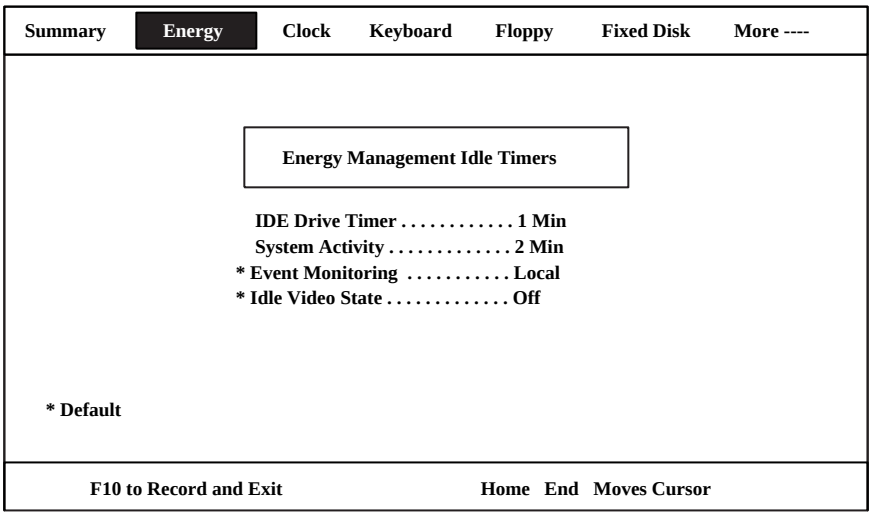


Figure 4-2: Energy Screen

Explanation

Options available on this screen enable the user to reduce power consumption when the system is idle.

Entry Fields

Field	Description	Parameters
IDE Drive Timer	This switch can be set to 1, 2, or 5 minutes. After this duration with no activity, the hard drive is spun down.	1. 1, 2 or 5 minutes.
System Activity	After the above time has elapsed with no activity, the system operating frequency is reduced to 8 or 16MHz depending upon the CPU.	1. 2, 5, 15, 30, 40, 60, 240 minutes.
Event Monitoring	"Local" corresponds to the keyboard input.	1. Local 2. Global
Idle Video State	When the system goes to slow speed operation, the screen blanks if this is set to "Off ."	1. On 2. Off

Table 4-2: Energy Screen Entry Fields

• Clock Screen

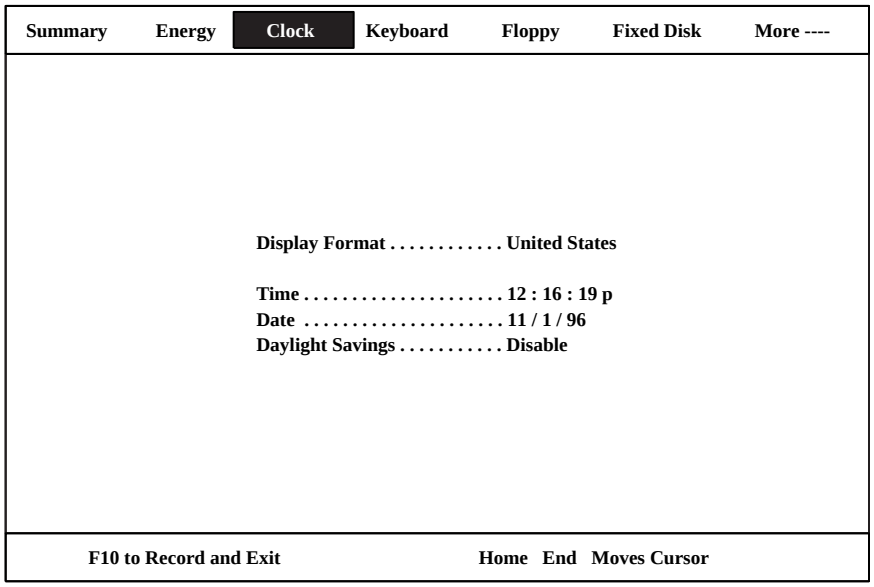


Figure 4-3: Clock Screen

Explanation

The time and date are maintained in the real-time clock (RTC). It's battery powered when the computer is shut off. The RTC needs to be set with the initial time/date. Adjustments are required periodically for continued accuracy. Variations in voltage (power supply or battery) and other technical issues make it impractical to tune the RTC with the same degree of precision as a dedicated timepiece.

To change the time or date, move the cursor into the field and press <Enter>. Enter the new data and press <Enter> again or <Esc>.

Entry Fields

Field	Description	Parameters
Display Format	Select the display format for time and date.	1. U.S. 2. International
Time	Press <Enter> and move the cursor under the number to change and enter "0-9" or "+" or "-".	1. 12hr am/pm 2. 24hr
Date	Press <Enter> and move the cursor under the number to change and enter "0-9" or "+" or "-".	1. mm/dd/yyyy 2. dd/mm/yyyy
Daylight Savings	The RTC can be instructed to automatically correct the time on the two daylight savings days of the year. Altering this field will not cause an immediate change. The RTC adjusts the time only when a daylight savings transition occurs.	1. Enable 2. Disable

Table 4-3: Clock Screen Entry Fields

• Keyboard Screen

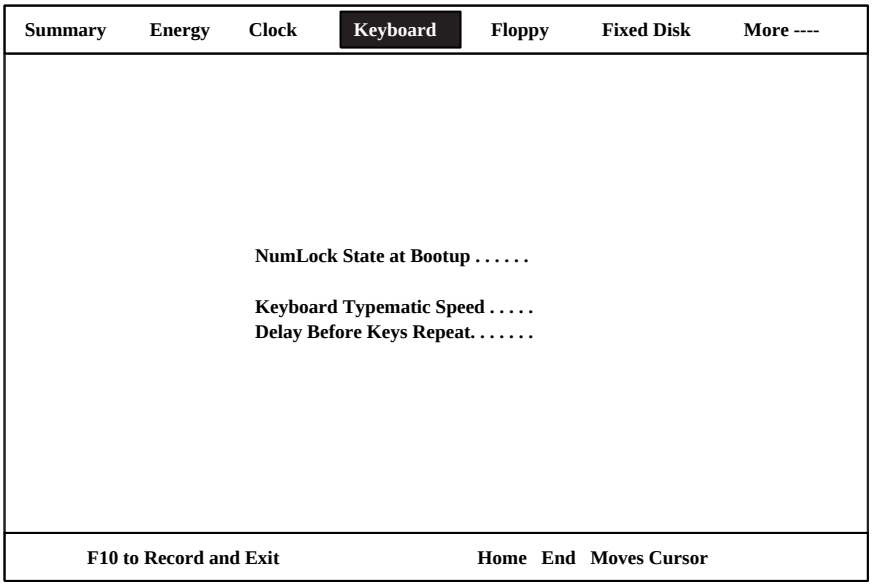


Figure 4-4: Keyboard Screen

Explanation

From this screen you can control the power-up state of NumLock, Keyboard Typematic Speed and Delay Before Repeat.

NumLock State at Bootup. This parameter sets the Numlock state of the numeric keypad of your keyboard at power-up. You can change it at any time by pressing the NumLock key.

When set to "Off," the numeric keys will produce special control functions (PgUp, PgDn, Home, End, Ins, Del, and cursors). When set to "On," the numeric keys will produce the indicated numbers.

Keyboard Typematic Speed. This is the rate in characters-per-second at which a key will repeat when depressed.

Delay Before Keys Repeat. This is the length of time a key can be depressed before it will begin to repeat.

Entry Fields

Field	Description	Parameters
NumLock State at Bootup	The initial NumLock state is programmable for cursor or numeric operation. "On" selects numeric entry and "Off" selects cursor control.	1. On 2. Off
Keyboard Typematic Speed	Select the default rate of 10cps or select from 2 cps to 30 cps.	1. Default 2. 2.0-30.0 cps
Delay Before Keys Repeat	Select one of four settings between 0.25 to 1.0 seconds that comfortably allows you to release the keys before they begin to repeat. **Note:** This field will display "Default" and cannot be changed if the "Keyboard Typematic Speed" field is set to "Default ."	1. Default 2. 0.25-1.0 sec

Table 4-4: Keyboard Screen Entry Fields

• Floppy Screen

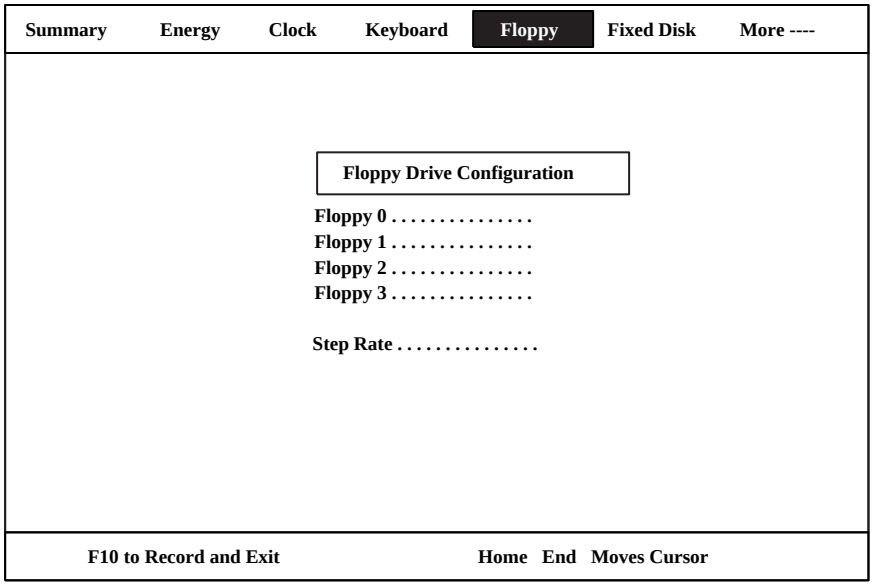


Figure 4-5: Floppy Screen

Explanation

Your system can have as many as four floppy disk drives, referred to as Floppy 0 through Floppy 3, corresponding to A:, B:, etc., respectively, depending on your operating system. Each floppy drive in your system must be identified as one of the following:

- 5／ 360K low density
- 3 fi 720K low density
- 5／ 1.2MB high density
- 3 fi 1.4MB high density
- 3 fi 2.8MB extra density

The BIOS will support:

2.88MB floppy drives, or

A second controller card, or

Four floppy drives.

Step Rate. This is the radial track-to-track speed of the recording heads.

Entry Fields

Field	Description	Parameters
Floppy 0 - 3	Indicate the drives present by specifying their types. Floppy 0 and Floppy 1 correspond to Drives A: and B:, respectively. The drive letters for Floppy 2 and 3 depend on your Operating System.	1. n/a 2. None 3. 5º, 360K 4. 3Ω, 720K 5. 5º, 1.2MB 6. 3Ω, 1.4MB 7. 3Ω, 2.88MB
Step Rate	Set to "Fast" for best performance. A "Slow" setting is provided for backward compatibility with 8MHz data transfer standards.	1. Fast 2. Slow

Table 4-5: Floppy Screen Entry Fields

• Fixed Disk Screen

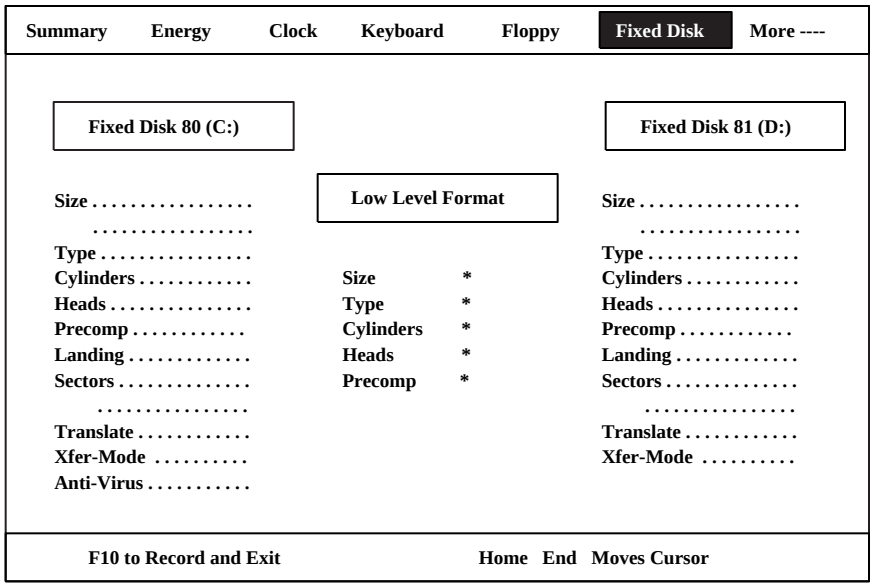


Figure 4-6: Fixed Disk Screen

Explanation

The Fixed Disk Screen allows you to define the hard disk drives on your system and to program the Low Level Format utility.

Fixed Disk 80 & 81. Fixed disks are referenced as Units 80 and 81, corresponding to C: and D:, depending on your operating system. The BIOS is unaware of any partitions or other logical mappings.

When you enter the fixed disk "Type" from 1 to 45, the system automatically enters the parameters. When you enter types 46 and 47, you can either enter the parameters from the documentation furnished with your drives or you can also enter a question mark (?) after entering 46 or 47. The BIOS will then enter the parameters directly from the disk.

Fixed disk parameters are sorted into a universal standard for fixed disk types. When the computer is booted, a table is constructed in main memory with these parameters. If your computer has Shadow RAM capability and the BIOS shadow is enabled, the table is generated in the EPROM image to assure 100% compatibility with all software.

NOTE: Novell 2.X requires the BIOS to be shadowed when using types 46 & 47.

Translate. If your fixed disk has more than 1024 cylinders, you can instruct the BIOS to translate the parameters. A drive with as many as 16K cylinders can be supported through this technique. Otherwise, the fixed disk interface is limited to the traditional 1K cylinders.

Anti-Virus. The Anti-Virus option offers a measure of protection against malicious programs which infect the main boot sector or low level format (destroy) your data. Since viruses often gain entry when an infected floppy disk is booted, you should supplement this defense with the "C: 1st" boot order in the Boot Sequence Utility.

NOTE: You will need to disable this option while using certain fixed disk maintenance programs (e.g., DOS FDISK), because their actions would be interpreted as a violation.

WARNING!

Many classes of viruses will not be detected, and even when a virus is detected, it may have already infected the disk, corrupted data, spread through a network, etc. Write protect the main boot sector by enabling this option. You will need to disable it prior to running fixed disk maintenance programs (e.g., FDISK). "No" writes to boot sector. "Yes" disallows writes to boot sector.

Entry Fields

Field	Description	Parameters
Size	This field is auto sensed.	1. None 2. MB capacity
Type	Scroll through 1-47 or enter numerically.	1. None 2. 1-45 3. 46 & 47
Cylinders Heads Precomp Landing Sectors	These fields are auto sensed When type 46 or 47 is entered, these fields can be edited.*	
Translate	A large drive, up to 16K cylinders, can be fully utilized by enabling BIOS translation. Otherwise, the traditional 1K cylinder interface is employed. "No" indicates 1K cylinders or less. "Yes" indicates more than 1K cylinders.	1. No 2. Yes
Xfer-Mode	**A = Standard** Data transfer is 1 sector per interrupt. **B = Poll** No interrupts. Strictly polls the drive for "ready." **C = Block** Transfers data based on the block size that the disk drive reports. **D = 32-Bit Block** Uses 32-bit instructions to transfer data.	1. A 2. B 3. C 4. D
Anti-Virus	Select "Yes" to enable.	1. No 2. Yes

Table 4-6: Fixed Disk Screen Entry Fields

*** NOTE: If your documentation does not indicate a Precomp value, you can make "None" appear by entering the same number as the Cylinders value. Similarly, if your documentation does not indicate a Landing Zone, use the same value as Cylinders.**

- VL-Bus IDE Screen

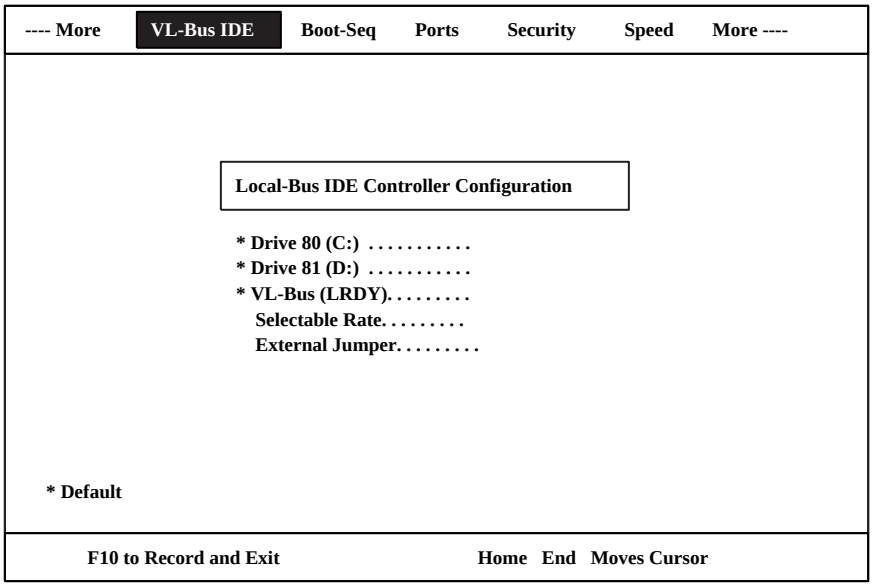


Figure 4-7: VL-Bus IDE Screen

Explanation

This screen allows you to get the maximum transfer rate possible from your IDE drives. When you enter a question mark (?) in the **Drive 80** field, the ATA rating reported by the drive will display in the bottom of the screen. By selecting “Selectable Rate” in the **Drive 80** field, you can then enter the rate shown on the screen in the **Selectable Rate** field. For two IDE drives, repeat the process for Drive 81. If you have only one IDE drive, select “External Jumper” in the Drive 81 field.

Entry Fields

Field	Description	Parameters
Drive 80 (C:) Drive 81 (D:)	Enter a question mark (?) to display the ATA rating of the drive in the bottom of the screen. Select "Selectable Rate" for any IDE drive present. Select "External Jumper" if no IDE drive is present.	1. Selectable Rate 2. External Jumper
VL-Bus (LRDY)	Select the ws access of the IDE controller. For example, if you're running at 50MHz, select "1ws ."	1. 0ws 2. 1ws
Selectable Rate	Enter the transfer rate displayed at the bottom of the screen when "?" is entered in a "Drive" field.	
External Jumper	CPU jumpers determine the transfer rate of the drive.	

Table 4-7: VL-Bus IDE Screen Entry Fields

- Boot Sequence Screen

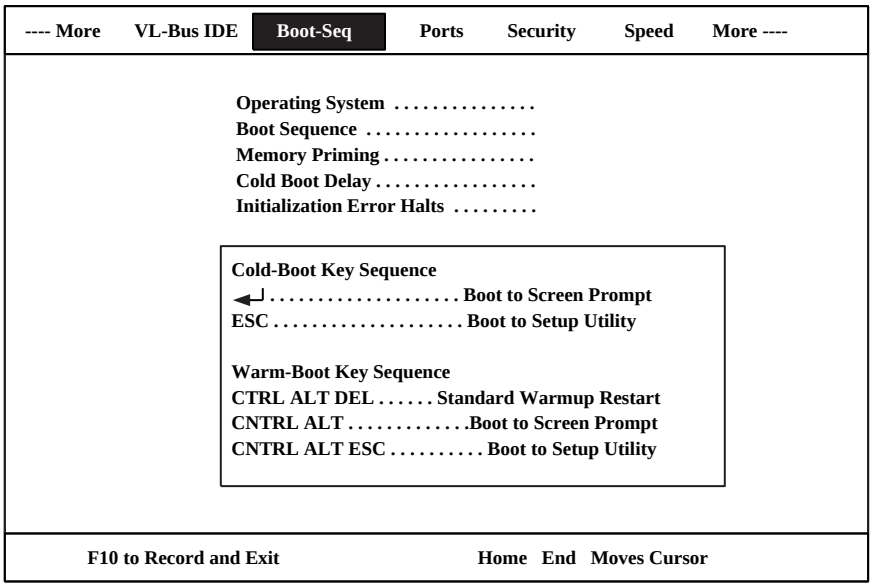


Figure 4-8: Boot Sequence Screen

Explanation

This utility allows you to configure your system's start-up functions.

Boot Sequence. The following four choices are provided:

- **A: 1st, C: 2nd.** This is an industry standard boot order where Drive C: is booted only when drive A: is empty.
- **C: 1st, A: 2nd.** Most installations use drive C: as the primary boot device. This eliminates the opportunity for a virus to enter your computer when a floppy is unintentionally left in the drive.
- **Auto-Search** instructs the system to first search the floppy drives, then the fixed disk drives to find a bootable system disk. If nothing is found, it displays a non-system disk error message. When it finds a bootable drive, it automatically makes it the primary boot device until you program it differently.
- **Screen Prompt** instructs the BIOS to pause and display a short menu that requests your selection of the boot drive, A: or C:.

NOTE: A prompted boot can also be invoked by pressing <Ctrl> + <Alt> + <Enter> during runtime or by pressing <Enter> during the cold boot memory test. (This is a convenient way to occasionally boot from floppy when the "C: 1st" order is selected here as the default). The following prompt will appear:

```
Press F1 to Boot A:, F2 to Boot C:
```

Respond by pressing <A> or <F1> to boot from floppy, or press <C> or <F2> to boot from the fixed disk.

Memory Priming. During cold boot, BIOS conducts a memory test that both initializes and verifies the entire memory subsystem. In systems with a large memory capacity, boot speed can be significantly increased by selecting Quick Scan to clear the memory.

Cold Boot Delay can provide additional power-up time required by some slow mechanical devices (e.g., fixed disks). A delay before Power On Self Test (POST) may be needed to allow proper initialization of various slow mechanical devices. This is especially true of certain IDE drives that are unprepared for the unusually swift execution of this BIOS. If you experience powerup difficulties, try a delay of 1 to 30 seconds.

Entry Fields

Field	Description	Parameters
Operating System	Select "OS/2" if the system is running the OS/2 operating system.	1. Not OS/2 2. OS/2
Boot Sequence	Specify the drive order used to load the Operating System.	1. A: 1st, C: 2nd 2. C: 1st, A: 2nd 3. Auto-Search 4. Screen Prompt
Memory Priming	Specify the memory testing method.	1. Full Test 2. Quick Scan
Cold Boot Delay	Unless required, select "None" to avoid an unnecessary delay.	1. None 2. 5 Sec
Initialization Error Halts	Select "Active" to enable.	1. Active 2. Inactive

Table 4-8: Boot Sequence Screen Entry Fields

- Security Screen

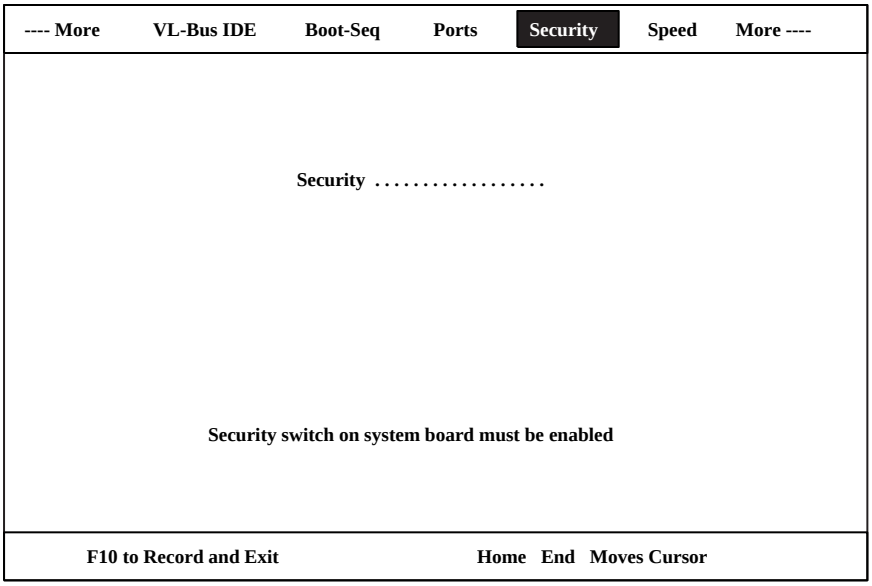


Figure 4-9: Security Screen

Explanation

A jumper must be installed on J19 before you can change or access the security password function. Once the jumper is installed, you can select a security code or password, which you must then enter to access the computer.

The message, **"Security Switch on system board must be enabled,"** displays at the bottom of the screen when "Disable" appears in the entry field. It reminds you the jumper must be installed before you can enter this field.

When the jumper is installed, setting the entry field to "Powerup/Setup" allows you to select a security code or password. You will then be prompted to enter your password on this screen and to verify it. You are also given the option of selecting "Setup Only," "Disable," or "Change Code."

"Setup only" allows you to view the Summary Screen without allowing you to change anything in Setup. "Disable" allows you to enter the computer without a password and "Change code" allows you to change your password once you've assigned it.

When you assign a security code, you are required to enter it when the computer boots and again on the Summary Screen in order to enter the Setup Utility.

Entry Fields

Field	Description	Parameters
Security	Select the security option desired.	1. Disable 2. Power/ Setup 3. Setup only 4. Change code

Table 4-9: Security Screen Entry Fields

- Speed Screen

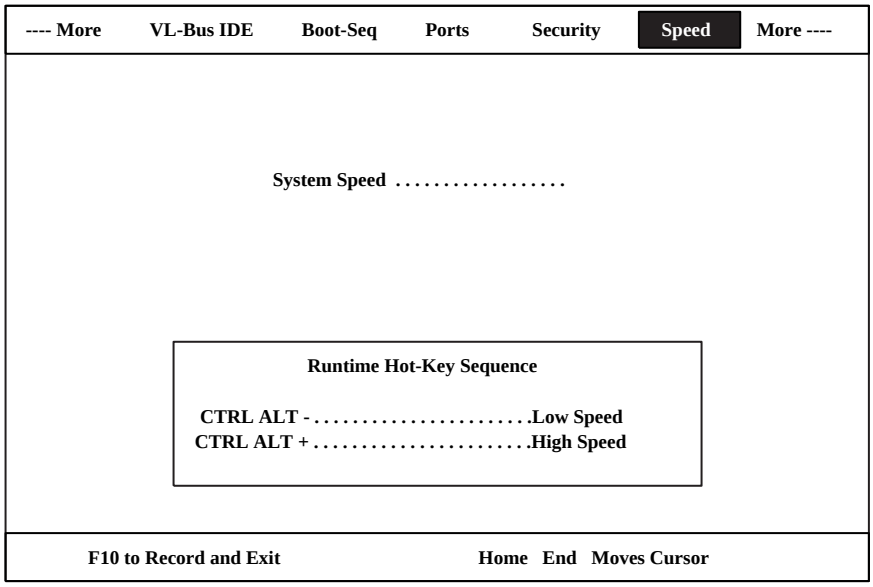


Figure 4-10: Speed Screen

Explanation

The operating speed of the CPU is configured here. High speed (turbo) will maximize the system performance. Low speed reduces performance to simulate the original, slower personal computers. You can change the speed during normal runtime by pressing <Ctrl> + <Alt> + <+> for High speed or <Ctrl> + <Alt> + <-> for Low speed.

Entry Fields

Field	Description	Parameters
System Speed	Select the computer's operating speed according to your preference.	1. Low 2. High

Table 4-10: Speed Screen Entry Fields

• Cache Screen

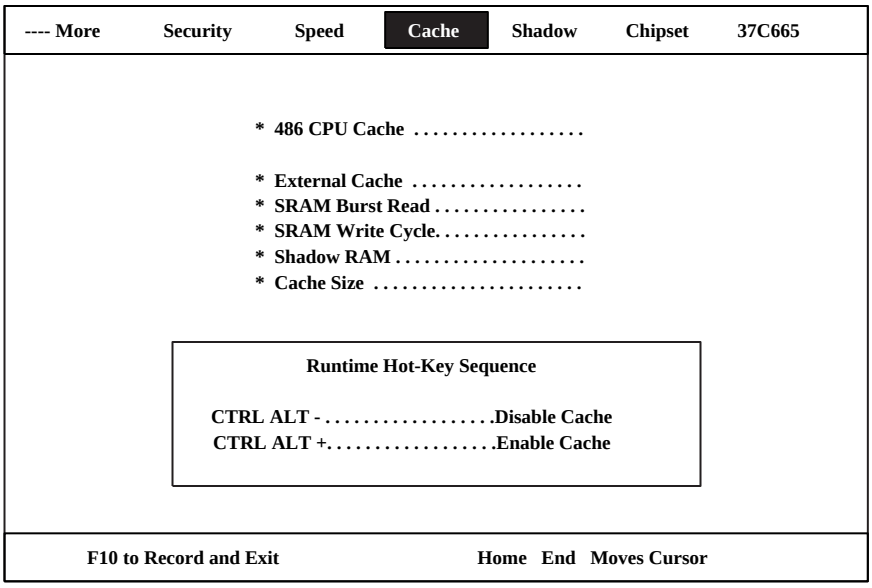


Figure 4-11: Cache Screen

Explanation

The purpose of a cache is to optimize system performance by increasing throughput of the memory subsystem. This is achieved through the use of a small quantity of Static RAM (SRAM). As data is fetched from slower main memory, it is copied into the faster SRAM. Subsequent references to this data are directed to the SRAM, occurring more swiftly than is possible from main memory.

The main objective of this utility is to allow you to enable the cache(s) in your system. As a general rule, you will obtain best results by making all memory present in your computer cacheable, disabling any non-cache blocks, and selecting the most aggressive timing parameters.

Non-cache blocks are used if a component or program in the system needs to have a non-cached memory area. The address of the non-cached block can start in the beginning of the base memory all the way to the end of the available memory.

Entry Fields

Field	Description	Parameters
486 CPU Cache	The cache can be enabled or disabled in this field.	1. Enable 2. Disable
External Cache	Indicates the amount of SRAM in the cache. Usually, BIOS detects this value automatically.	1. None 2. Enable 3. Disable
SRAM Burst Read	Indicates the number of wait states per cache read access.	1. 0ws 2. 1ws
SRAM Write Cycle	Indicates the number of wait states per cache write access.	1. 0ws 2. 1ws
Shadow RAM	Shadow RAM is either cacheable or non-cacheable.	1. Enable Cache 2. Disable Cache
Cache Size	The BIOS enters this number automatically.	

Table 4-11: Cache Screen Entry Fields

• Shadow RAM Screen

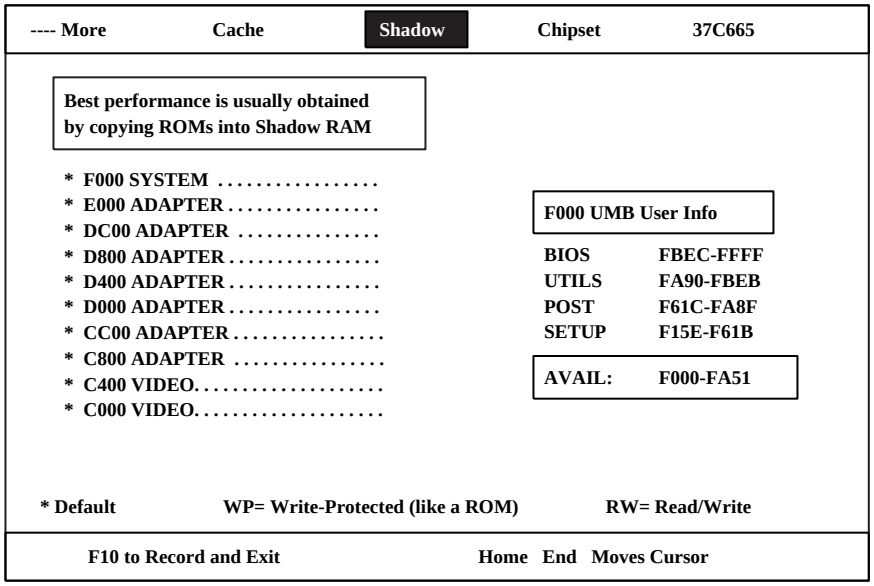


Figure 4-12: Shadow RAM Screen

Explanation

Shadow RAM is a mechanism that copies Read Only Memory into main memory, then substitutes that memory image for the original ROM. This increases the execution speed of programming that resides in ROM. BIOS and VGA Adapters are two main examples of ROMs that demonstrate significant performance gains when they are shadowed.

Since ROMs are by definition Read-Only, it is usually desirable to write protect the Shadow RAM. However, Shadow RAM can also be used as general purpose memory by certain programs. In this case, it should be enabled as Read-Write memory. While most Adapter ROMs can be shadowed either way, some permit only the RW or WP option, and a rare few cannot be shadowed at all. You may need to experiment a little.

Unshadowed segments display "Vacant" if no adapter ROM is present there. Unshadowed segments containing a ROM will indicate ROM #n, where n is a number from 0 through 9. Each ROM is assigned a unique number. If a single ROM spans several segments, then the same ROM #n will appear multiple times. ROM #0 is always the system BIOS.

Shadow RAM is obtained from a gap in the otherwise contiguous memory space of the computer. The 384K region between the 640K and 1MB boundaries is occupied not by memory, but instead by ROMs, video memory, and possibly other system-level devices. The memory that should appear there is simply inaccessible and unused. One way to make use of this lost memory is to activate it as Shadow RAM. Certain designs can also remap a portion of this 384K into the Extended Memory pool, provided it is not already enabled as Shadow RAM. In most designs with this capability, remap will be prevented if any Shadow segment is enabled in the D000 through E000 regions. View the Extended Memory field in the Summary screen to see how (or if) a particular Shadow configuration affects your computer's memory.

The critical runtime programming in the BIOS section cannot be assigned to UMB space. The UTILS section should not be assigned to UMBs either, since the speed and cache hotkey functions <Ctr>l+<Alt>+<+> and <Ctrl>+<Alt>+<-> are contained in this section. Both the POST and SETUP regions may always be reclaimed for UMBs since they contain only power-up and boot time code. The AVAIL field shows the entire recommended range beginning at the bottom of the F000 EPROM.

Field	Description	Parameters
F000 System	The system BIOS occupies this 64K segment. For best results, always enable "WP-Shadow" here.*	1. ROM # 2. WP-Shadow
C800 through E000 Adapter	If present, Adapter ROMs for non-video devices (e.g., disk controllers or LAN adapters) are found in one or more of these seven segments. While C800-DC00 are 16K segments, E000 is 64K.	1. Vacant 2. RW-Shadow 3. ROM #2
C000 & C400 Video	Video Adapter ROMs (e.g., VGA) usually occupy both of these 16K segments. They appear collectively as ROM #1 when shadow is disabled. Best performance is usually obtained when shadow is enabled here.	1. ROM #1 2. WP-Shadow

Entry Fields

Table 4-12: Shadow RAM Screen Entry Fields

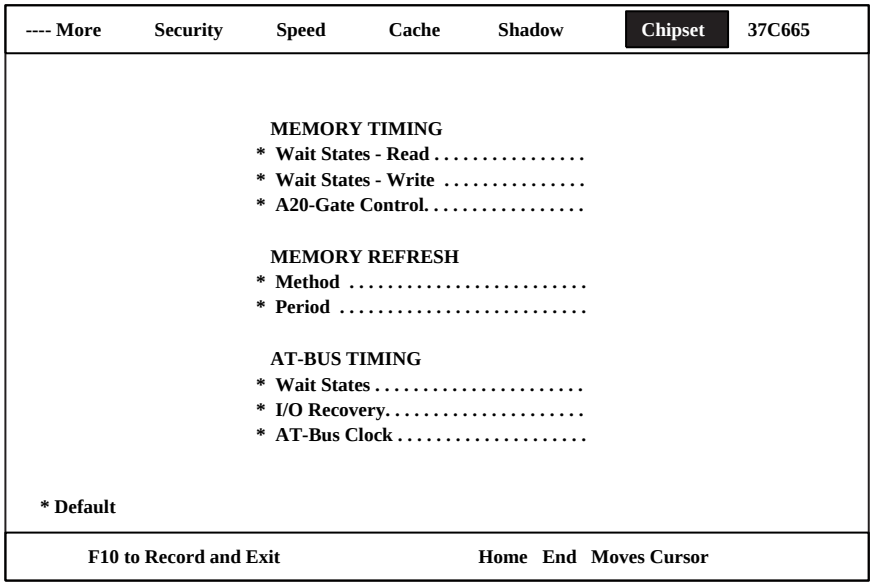
* Fixed Disk Types 46 & 47 can be used with Novell 2.X only when F000 is shadowed.

F000 UMB (Upper Memory Block) User Info. This region of memory is traditionally reserved for BIOS and ROMs. A maximum of 640K can be installed as Base Memory. Various Memory Manager programs are able to increase the Base Memory by reclaiming unused gaps between the 640K and 1 MB boundaries.

Approximately the bottom 3/4 of the BIOS EPROM contains expendable code that may be reclaimed as UMB space. A view only breakdown of its content appears on this Setup screen for your convenient reference. You will need to furnish this information to your Memory Manager software in order to create a UMB in the F000 BIOS region.

BIOS . . . . Fzzz-FFFF	vital runtime BIOS
UTILS . . . Fyyy-Fzzz	speed & cache on/off
POST . . . . Fxxx-Fyyy	power-up code
SETUP . . Fwww-Fxxx	Setup Utility
AVAIL . . . Fzzz-Fyyy	available for UMBs

NOTE: The actual values entered for “w, x, y and z” will vary depending upon the BIOS version.



- Chipset Screen

Figure 4-13: Chipset Screen

Explanation

This utility permits optional fine tuning of certain chipset parameters that are very technical in nature.

In modern ISA designs, practically the entire system logic is contained in a few large chips called the chipset. Its primary responsibility is to service and maintain the CPU and associated logic circuits.

The chipset is typically programmable by BIOS, allowing it to be adapted to a broad range of designs and operating environments. Most chipset functions are presented elsewhere in the Setup Utility as standard BIOS features. The more technical core logic functions, including Memory and AT-Bus timing, are managed here.

Field	Description	Parameters
MEMORY TIMING		
Wait States - Read	Specified in terms of "wait states" or ns rating (nanosecond). Numerically lower "ws" values and ns values cause faster access giving better performance. Common ns values range from 60 to 100ns and common "ws" values are 1 - 2.	1. 1.0 - 2.0ws 2. 60 - 100ns
Wait States - Write	Specified in terms of "wait states" or ns rating (nanosecond). See above.	1. 0 - 1ws 2. 60 - 100ns
A20-Gate Control	General system failure during Protected Mode programs (e.g., Windows, OS/2, or EMS drivers) may be correctable by keeping the A20-Gate Enabled. To do so, set this field to "Always On." Set this field to "Normal" for standard A20 handling.	1. Normal 2. Always On
MEMORY REFRESH		
Method	"Standard" refresh synchronizes the AT Bus memory refresh and the on-board memory refresh. "Hidden" refresh decouples these two to refresh them independently.	1. Standard 2. Hidden
Period	Specified in terms of μs rating (microsecond).	1. 15 μs 2. 60 μs
AT-BUS TIMING		
Wait States	Many AT-Bus devices (especially IDE drives) require an extra delay between back-to-back cycles when running with an increased AT-Bus clock or in a high speed system.	1. Normal 2. Extra
I/O Recovery	A delay state between back-to-back I/O cycles.	1. Normal 2. Extra
AT-Bus Clock	The normal "dropout" rate for peripherals is 11 MHz. It is possible to operate the Orca board at 11 MHz, but it will involve finding expansion cards that will operate at that speed. The speed selected will affect all I/O transmissions. In systems set to run without any additional cards (network, video, controllers, modems), the Orca can run at the highest available speed. Default is 8.3 MHz.	1. 8.3 MHz 2. 11.1 MHz 3. 14.3/2 MHz 4. 5.6 MHz 5. 6.7 MHz

Entry Fields

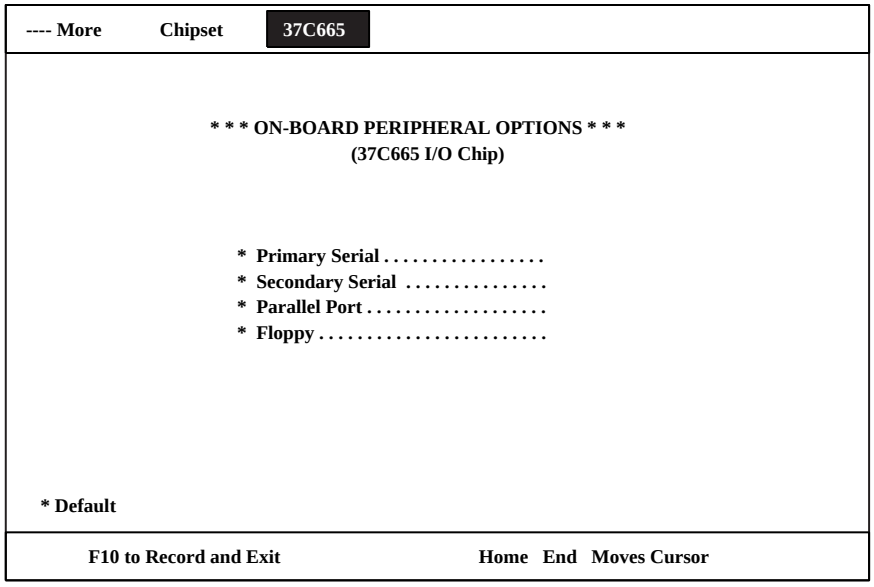


Table 4-13: Chipset Screen Entry Fields

- 37C665 Screen

Figure 4-14: 37C665 Screen

Explanation

The 37C665 Multifunction Controller (XIO) provides two serial ports, one parallel port, an IDE interface, and a floppy disk controller. The controller determines the address to respond to and the IRQ to use for each port.

NOTE: If you use an external I/O card, you must disable the Floppy field on this screen. To disable the internal IDE, you must place a jumper on pins 4 and 6 on J11.

Field	Description	Parameters
Primary Serial	When the port is set to "Auto," the BIOS looks for ports on the backplane first, then on the CPU board. The port can also either be disabled or it can be identified as a specific port.	1. Auto 2. COM1- 4 3. Disable
Secondary Serial	When the port is set to "Auto," the BIOS looks for ports on the backplane first, then on the CPU board. The port can also either be disabled or it can be identified as a specific port.	1. Auto 2. COM1- 4 3. Disable
Parallel Port	When the port is set to "Auto," the BIOS looks for ports on the backplane first, then on the CPU board. The port can also either be disabled or it can be identified as a specific port.	1. Auto 2. Video (3BC) 3. LPT1 (378) 4. LPT2 (278) 5. Disable
Floppy	The floppy drive can be enabled or disabled.	1. Enable 2. Disable

Entry Fields

Table 4-14: 37C665 Screen Entry Fields

Post Code #	State
00	Cold Start
01	Hook 00, Custom 8042
02	Disable critical I/O, Reset DMA/FDC
03	Checksum EPROM
04	Test Page Registers/Page Register Boot
05	Keyboard controller self test, Enable A20 gate
06	Initialize ISA I/O
07	Hook 01
08	Refresh toggle test
09	Test DMA master/slave registers
0A	Test base 64K memory
0B	Test interrupt controller mask
0C	Test interrupt controllers and initialize interrupt vectors
0D	Test 8254 timer
0E	Test speaker channel
0F	Test Real Time Clock
10	Hook Video
11	Test CMOS memory/battery
12	Display signon message
14	Size and test base memory
15	Retry keyboard initialization
16	Size and test cache
17	Test A20 gate
18	Size extended memory, check for Stuck NMI
19	Size system memory
1A	Test real time clock
1B	Determine Comm. Ports
1C	Print screen vector
1D	Initialize numeric coprocessor
1E	Determine FDC type
1F	Determine IDE type
20	Check CMOS for FDC/FIXED type
21	Keyboard locked
22	Setup numlock, check security
23	Final port setup
24	Set keyboard typematic rate
25	Initialize floppy disk drive
26	Initialize fixed disk
27	Clear screen and set mode for primary video adapter
28	Hook 06
29	Setup 64K segments
2A	Adapter checksums
2B	Enable NMI
2C	Reserved
2D	Reserved
2E	Interrupt 19H
2F	Boot OS

Table 4-15: Orca Post Codes

Post Code #	State
32	Test CPU Burst
33	Power management - warm boot disable
34	Determine 8042 type
35	Test High Memory Wrap-around
36	Determine CPU
37	Validate CPU
38	Green PC setup
39	Reserved
3A	Reserved
3B	Reserved
3C	Set OEM defaults for bridge
3D	Identify AT-BUS CDE space
3E	Reserved
3F	Reserved
40	ATA mode support
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Determine PS/2 mouse
46	Reserved
47	Reserved
48	Setup Utility

Table 4-15: Orca Post Codes (continued)

00/00H	Cold-Boot commences. (Not seen with warm-boot).
01/01H	Hook 00. OEM specific
02/02H	Disable critical I/O: 6845s
03/03H	BIOS checksum test.
04/04H	Page register test. (Ports 818F).
05/05H	8042 (Keyboard Controller) Self test.
06/06H	Gang Port Init: 8237 m/s
07/07H	Hook 01. OEM specific
08/08H	Refresh toggle test (PORTB).
09/09H	Pattern test master/slave 8237s
10/0A H	Base 64K memory test.
11/0B H	Pattern test master/slave 8259 mask regs.
12/0C H	8259 / IRQ tests
13/0D H	8254 channel0 test and initialization.
14/0E H	8254 channel2 toggle test
15/0F H	RTC tests/inits: Init REGB
19/13H	Hook 02. OEM specific
16/10H	Video Initialization.
17/11H	CMOS Checksum test.
18/12H	Sign on message
20/14H	Size/Test base memory (low 64K already done)
21/15H	Perform 2nd try KB init
22/16H	Hook 03. OEM specific. Size/Test cache.
23/17H	Test A20 gate
24/18H	Size/Test extended memory
25/19H	Hook 04 and Size/Test system memory ("special" OEM memory).
26/1A H	Test RTC Update In Progress and validate time.
27/1B H	Serial port determination
28/1C H	Parallel port determination
29/1D H	Coprocessor determination/initialization.
30/1E H	Floppy controller test/determination
31/1FH	Fixed Disk controller test/determination
32/20H	Rigorous CMOS parameter validation
33/21H	Front Panel lock check
34/22H	Set NumLock
35/23H	Hook 05. OEM specific.
36/24H	Set typematic rate.
40/28H	Hook 06. OEM specific
37/25H	Floppy subsystem initialization.
38/26H	Fixed subsystem initialization.
39/27H	ACK errors
41/29H	Disable A20 gate
42/2A H	ACK errors
43/2B H	Enable parity checking and NMI.
44/2C H	Install E000 ROM.
45/2D H	ACK errors.
46/2E H	Hook 07. OEM specific. Login EMS (if built in).
47/2FH	Pass control to INT19 (boot disk).

Table 4-16: Diagnostic Port 80h Post Codes

Port 80H	Beep Code	Error Message
03/03H	LHLLL	ROMBIOS Checksum Failure
04/04H	LHHLL	DMA Page Register Failure
05/05H	LHLHL	Keyboard Controller Selftest Failure
07/07H	LHHHL	Memory Refresh Circuitry Failure
08/08H	LHLLH	Master (16 bit) DMA Controller Failure
08/08H	LHHLH	Slave (8 bit) DMA Controller Failure
10/0AH	LHLLLL	Memory Bank 0 Pattern Test Failure
10/0AH	LHHLLL	Memory Bank 0 Parity Circuitry Failure
10/0AH	LHLHLL	Memory Bank 0 Parity Error
10/0AH	LHHHLL	Memory Bank 0 Data Bus Failure
10/0AH	LHLLHL	Memory Bank 0 Address Bus Failure
10/0AH	LHHLHL	Memory Bank 0 Block Access Read Failure
10/0AH	LHLHHL	Mem. Bank 0 Block Access Read/Write Failure
11/0BH	LHHHHL	Master 8259 (Port 21) Failure
11/0BH	LHLLLH	Slave 8259 (Port A1) Failure
12/0CH	LHHLLH	Master 8259 (Port 20) Interrupt address Error
12/0CH	LHLHLH	Slave 8259 (Port A0) Interrupt Address Error
12/0CH	LHHHLH	8259 (Port 20/A0) Interrupt Address Error
12/0CH	LHLLHH	Master 8259 (Port 20) Stuck Interrupt Error
12/0CH	LHHLHH	Slave 8259 (Port A0) Stuck Interrupt Error
12/0CH	LHLHHH	System Timer 8254 CH0/IRQ0 Interrupt Failure
13/0DH	LHHHHH	8254 Channel 0 (System Timer) Failure
14/0EH	LHLLLLH	8254 Channel 2 (Speaker) Failure
14/0EH	LHHLLLH	8254 OUT2 (Speaker Detect) Failure
15/0FH	LHLHLLH	CMOS RAM Read/Write Test Failure
15/0FH	LHHHLLH	RTC Periodic Interrupt / IRQ8 Failure
16/10H	LHLLHLH	Video ROM Checksum Failure at Address XXXX Mono Card Memory Error at Address XXXX Mono Card Mem. Address Line Error at Address XXXX Color Graphics Card Memory Error at Address XXXX Color Graphics Card Address Line Error Address XXXX
17/11H	None	Real Time Clock (RTC) Battery is Discharged
17/11H	None	Battery Backed Memory (CMOS) is Corrupt
18/12H	LHHLHLH	Keyboard Controller Failure
20/14H		
24/18H		
25/19H	LHLHHLH	Memory Parity Error
20/14H		

Table 4-17: Beep Codes and Error Messages

Beep Codes L = low tone and H = high tone

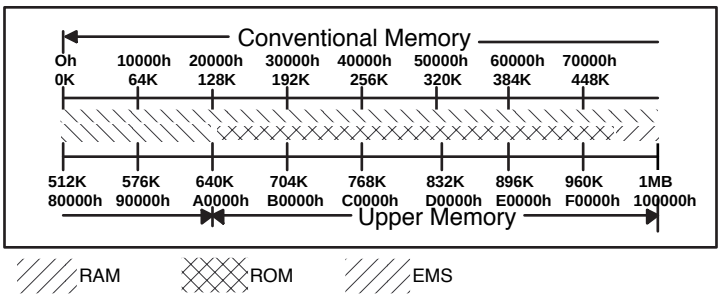
Port 80H	Beep Code	Error Message
24/18H		
25/19H	LHHHHLH	I/O Channel Error
20/14H		
24/18H		
25/19H	None	RAM Pattern Test Failed at XXXX
		Parity Circuit Failure in Bank XXXX
		Data Bus Test Failed: Address XXXX
		Address Line Test Failed at XXXX
		Block Access Read Failure at Address XXXX
		Block Access Read/Write Failure: Address XXXX
		Banks Decode to Same Loc.: XXXX & YYYY
18/12H		
21/15H	None	Keyboard Error Stuck Key
		Keyboard Failure or no Keyboard Present
23/17H	LHLLLHH	A20 Test Failure Due to 8042 Timeout
23/17H	LHHLLHH	A20 Gate Stuck in Disabled State (A20=0)
23/17H	None	A20 Gate Stuck in Asserted State (A20 Follows CPU)
26/1AH	LHLHLHH	Real Time Clock (RTC) is Not Updating
26/1AH	None	Real Time Clock (RTC) Settings are Invalid
30/1EH	None	Diskette CMOS Configuration is Invalid
		Diskette Controller Failure
		Diskette Drive A: Failure
		Diskette Drive B: Failure
31/1FH	None	Fixed Disk CMOS Configuration is Invalid
		Fixed Disk C: (80) Failure
		Fixed Disk D: (81) Failure
		Please Wait for Fixed Disk to Spin Up
		32/Diskette Configuration Change20H, (None), Fixed Disk Configuration Chg.
		Serial Port Configuration Change
		Parallel Port Configuration Change
		Video Configuration Change
		Memory Configuration Change
		Numeric Coprocessor Configuration Change
33/21H	None	System Key is in Locked Position Turn Key to Unlocked Position
41/29H	None	Adapter ROM Checksum Failure at Address XXXX

Table 4-17: Beep Codes and Error Messages (continued)

Beep Codes L = low tone and H = high tone

Type	Size (MB)	Cylinder	Heads	Precomp	Landing Zone	Sectors/ Track
1	10.7	306	4	128	305	17
2	21.4	615	4	300	615	17
3	32.1	615	6	300	615	17
4	65.5	940	8	512	940	17
5	49.1	940	6	512	940	17
6	21.4	615	4	None	615	17
7	32.2	462	8	256	511	17
8	31.9	733	5	None	733	17
9	117.5	900	15	None	901	17
10	21.4	820	3	None	820	17
11	37.2	855	5	None	855	17
12	52.1	855	7	None	855	17
13	21.3	306	8	128	319	17
14	44.7	733	7	None	733	17
15	0.0	0	0	None	0	0
16	21.3	612	4	0	663	17
17	42.5	977	5	300	977	17
18	59.5	977	7	None	977	17
19	62.4	1024	7	512	1023	17
20	31.9	733	5	300	732	17
21	44.7	733	7	300	732	17
22	21.9	733	5	300	733	17
23	10.7	306	4	0	336	17
24	42.9	805	4	None	805	26
25	72.5	925	9	None	925	17
26	104.9	776	8	None	776	33
27	44.6	1024	5	512	1024	17
28	71.3	1024	8	None	1023	17
29	71.6	823	10	None	823	17
30	159.8	1224	15	None	1223	17
31	98.0	1024	11	None	1024	17
32	133.7	1024	15	None	1024	17
33	44.6	1024	5	None	1024	17
34	10.7	612	2	128	612	17
35	80.2	1024	9	None	1024	17
36	71.3	1024	8	512	1024	17
37	42.8	615	8	128	615	17
38	71.6	823	10	256	823	17
39	42.2	809	6	128	809	17
40	42.8	820	6	None	820	17
41	42.5	977	5	None	977	17
42	42.7	981	5	None	981	17
43	71.6	823	10	512	823	17
44	72.2	830	10	None	830	17
45	119.7	917	15	None	917	17

Table 4-18: Fixed Disk Parameters



BIOS	FFFF:F
BIOS	F800:0
Could be Page Frame for EMS	F000:0
Could be Page Frame for EMS	E800:0
	E000:0
Network Cards often use this area.	D800:0
Hard Drive ROMs	D000:0
EGA/VGA ROM	C800:0
CGA/RAM EGA/VGA Text Modes	C000:0
MONO/RAM	B800:0
EGA/VGA RAM Graphics Modes	B000:0
EGA/VGA RAM Graphics Modes	A800:0
640K Base	A000:0
Interrupt Vector Table	0040:0
	0000:0

Table 4-19: Memory Map

Q & A

This section contains questions that are most frequently asked of our Customer Support Department about the BIOS setup utility. You may be able to diagnose any difficulty you have by referring to them prior to calling our Customer Support.

Q1 How do you setup the board in the extended setup?

A1 Try using the defaults first (defaults have an asterisk at the beginning of the line item).

A2 Set the COM ports, IDE and Floppy for enabled or disabled, as needed.

A3 The defaults are:

Read cycle wait states:	2
Write cycle wait states:	3
Refresh:	Normal
AT wait cycle wait states:	0
Video BIOS:	Non-cacheable
SRAM wait states:	1
Non-cacheable blocks 1 & 2:	Disabled

Q2 What are the non-cacheable blocks for?

A These are used if a component or program in the system needs to have non cached memory area.

Q3 What is the starting address for these non-cacheable blocks?

A The non-cacheable block can start in the beginning of the base memory all the way to the end of the available memory. The largest block size is 412k times two (non-cache blocks 1 and 2).

Q4 Do I have to use the on board IDE or floppy disk controllers?

A No.

Q5 Do you have to use the serial or parallel ports built onto the CPUs?

A No, you may relocate or disable them.

Q6 What if you are using a different controller other than the one built into the CPU?

A This is not a problem if you adjust the BIOS to use an off-board controller.

Q7 Can I use a SCSI controller and where should I set the address?

A1 You can use a SCSI controller. You must set the card address for the primary controller in the system. Then find an available appropriate address to set the SCSI BIOS to.

A2 YOU MUST DISABLE THE ON-BOARD IDE CONTROLLER IF YOU WANT THE SCSI CONTROLLER TO BE THE BOOT DEVICE.)

Q8 Can I use an ESDI controller and where should I set the address?

A1 You can use an ESDI controller. The address should be set for the primary controller in the system. Then find an available appropriate address to set the ESDI BIOS to.

A2 YOU MUST DISABLE THE ON-BOARD IDE CONTROLLER IF YOU WANT THE ESDI CONTROLLER TO BE THE BOOT DEVICE.

Q9 What preventive maintenance steps can I take?

A Ensure all fans in the chassis are working.

Clean the filter with warm water or compressed air.

Replace brittle or torn filters.

Allow ample air circulation behind the chassis.

Keep all cables free from tangles.

CAUTION!

Electrostatic Discharge (ESD) may damage memory chips, programmed devices and other electrical components. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat. Grounding can also occur by touching a chassis that is plugged into a power outlet.

Appendix 1 Technical Reference

Standard PC-AT I/O Map

Address (Hex)	Device
000 - 01F	DMA Controller
020 - 03F	Interrupt Controller 1
040 - 05F	Timer
060 - 06F	Keyboard Controller
070 - 07F	Real Time Clock (non-maskable interrupt)
080 - 09F	DMA Page Registers
0A0 - 0BF	Interrupt Controller 2
0C0 - 0DF	DMA Controller 2
0F8 - 0FF	Math Co-processor
1F0 - 1FF	Hard Disk Controller
200 - 207	Game I/O
278 - 27F	Prototype Card
2F8 - 2FF	Serial Port 2
300 - 31F	Prototype Card
360 - 36F	(Reserved)
378 - 37F	Parallel Printer Port
380 - 38F	SDLC Bisynchronous 2
3A0 - 3AF	Bisynchronous 1
3B0 - 3BF	Monochrome Display/Printer
3C0 - 3CF	(Reserved)
3D0 - 3DF	Color Graphics Display Adapter
3F0 - 3F7	Floppy Disk
3F8 - 3FF	Serial Port COM1

Table A1-1: Standard PC-AT I/O Map

DMA Channel Page Register and I/O Addresses

Controller 1: 8-bit (ports 000-00F)	
Page Register	**I/O Hex Address**
Channel 0	087
Channel 1	083
Channel 2	081
Channel 3	082
Controller 2: 16-bit (AT Only - ports 0C0-0DF)	
Channel 5	08B
Channel 6	089
Channel 7	08A
Refresh (AT)	08F

Table A1-2: DMA Channel Page Register and I/O Addresses

DMA Channel Assignments

Channel	Function
0	Reserved
1	SDLC
2	Floppy Disk
3	Spare
4	Cascade for CTRL
5	Spare (Reserved)
6	Spare (Reserved)
7	Spare (Reserved)

Table A1-3: DMA Channel Assignments

DMA Controller Register Functions

DMA#		Description
1	2	
000	0C0	CH0 base and current address
001	0C2	CH0 base and current word count
002	0C4	CH1 base and current address
003	0C6	CH1 base and current word count
004	0C8	CH2 base and current address
005	0CA	CH2 base and current word count
006	0CC	CH3 base and current address
007	0CE	CH3 base and current word count
008	0D0	Read status register/write command register
009	0D2	Write request register
00A	0D4	Write single mask register bit
00B	0D6	Write mode register
00C	0D8	Clear byte pointer flip-flop
00D	0DA	Read temporary register/write master clear
00E	0DC	Clear mask register
00F	0DE	Write all mask register bits

Table A1-4: DMA Controller Register Functions

Channel	Name	Function
NMI	NMI	Parity
0	IRQ0	System Timer Output 0*
1	KYBIRQ	Keyboard Output Buffer Full
2	IRQ2	CTRL2 Interrupt (IRQ8 - IRQ15)
3	IRQ3	Serial Port 2 (COM2)
4	IRQ4	Serial Port 1 (COM1)
5	IRQ5	Parallel Port 2
6	IRQ6	Floppy Disk Controller
7	IRQ7	Parallel Port 1
8	RTCIRQ	Real Time Clock
9	IRQ9	Software redirected to INT 0Ah
10	IRQ10	External ISA Bus Device (Reserved)
11	IRQ11	External ISA Bus Device (Reserved)
12	IRQ12	External ISA Bus Device (Reserved)
13	IRQ13	Math Coprocessor
14	IRQ14	Hard Disk Controller
15	IRQ15	External ISA Bus Device (Reserved)

Table A1-5: Interrupts

* These interrupts exist on the system board and are not available on the ISA Bus Connectors.

CMOS RAM Address Map

Address	Description
00 - 0D	*Real Time clock information
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Floppy disk drive type byte - drives A & B
11	Reserved
12	Hard disk type byte - drives C & D
13	Reserved
14	Equipment byte
15	Low base memory size below 1 MB
16	High base memory size below 1 MB
17	Low expansion memory size above 1 MB
18	High expansion memory size above 1 MB
19 - 2D	Reserved
2E - 2F	Checksum for bytes 10 - 2D
30	*Low memory size determined by Pwr Up
31	*High memory size determined by Pwr Up
32	*BCD century byte
33	Information flags (set during power on)
34 - 3F	Reserved

Table A1-6: CMOS RAM Address Map

* These addresses are not verified by CHECKSUM.

Real-Time Clock Information (Addresses 00-0D)

Byte	Function	Address
0	Seconds	00
1	Seconds alarm	01
2	Minutes	02
3	Minutes alarm	03
4	Hours	04
5	Hours alarm	05
6	Day of week	06
7	Day of month	07
8	Month	08
9	Year	09
10	Status Register B	0A
11	Status Register C	0B
12	Status Register D	0C
13	Status Register E	0D

Table A1-7: Real-Time Clock Information

ISA Connector Pin Assignment

Pin #	Assign.	Pin #	Assign.	Pin #	Assign.	Pin #	Assign.
A01	IOCHCHK#	B01	GND	C01	SBHE#	D01	EMCS16#
A02	SD7	B02	RESETDRV	C02	LA23	D02	IOCS16#
A03	SD6	B03	+5 V	C03	LA22	D03	IRQ10
A04	SD5	B04	IRQ9	C04	LA21	D04	IRQ11
A05	SD4	B05	+5 V	C05	LA20	D05	IRQ12
A06	SD3	B06	DRQ2	C06	LA19	D06	IRQ15
A07	SD2	B07	-12 V	C07	LA18	D07	IRQ14
A08	SD1	B08	ENDXFR#	C08	LA17	D08	DACK0#
A09	SD0	B09	+12 V	C09	MEMR#	D09	DRQ0
A10	IOCHRDY	B10	GND	C10	MEMW#	D10	DACK5#
A11	AEN	B11	SMEMW#	C11	SD8	D11	DRQ5
A12	SA19	B12	SMEMR#	C12	SD9	D12	DACK6#
A13	SA18	B13	IOW#	C13	SD10	D13	DRQ6
A14	SA17	B14	IOR#	C14	SD11	D14	DACK7#
A15	SA16	B15	DACK3#	C15	SD12	D15	DRQ7
A16	SA15	B16	DRQ3	C16	SD13	D16	+5 V
A17	SA14	B17	DACK1#	C17	SD14	D17	MASTER#
A18	SA13	B18	DRQ1	C18	SD15	D18	GND
A19	SA12	B19	REFRSH#				
A20	SA11	B20	SYSCLK				
A21	SA10	B21	IRQ7				
A22	SA9	B22	IRQ6				
A23	SA8	B23	IRQ5				
A24	SA7	B24	IRQ4				
A25	SA6	B25	IRQ3				
A26	SA5	B26	DACK2#				
A27	SA4	B27	TC				
A28	SA3	B28	BALE				
A29	SA2	B29	+5 V				
A30	SA1	B30	OSC				
A31	SA0	B31	GND				

Table A1-8: ISA Connector Pin Assignments

Appendix 2 Glossary of Terms

B

bidirectional parallel port: An eight-bit port that can be used for an input as well as an output device.

BIOS (Basic Input/Output System): The on-board firmware which communicates with the display, keyboard, printers and other peripheral devices.

bus: A common pathway, or channel, between multiple devices consisting of one or more electrical conductors that transmit power or binary data to the various sections of a computer.

C

cache: A collection of the most recently accessed data or instructions.

CMOS (Complementary Metal Oxide Semiconductor): A technique of using PMOS and NMOS transistors in a complementary fashion where power is consumed only during the switching phase. With the input statically high or low, the power dissipation is essentially zero.

CMOS RAM: Random Access Memory made from CMOS transistors.

D

DMA (Direct Memory Access Channel): A channel for transferring data from host main memory to and from peripherals without direct involvement of the CPU resources.

DRAM (Dynamic Random Access Memory): The main memory in your computer. It needs to be refreshed by a memory controller or it will lose its information.

Appendix 2 Glossary of Terms

E

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power. The information can be erased and new information written.

F

flash BIOS: BIOS that is stored in flash memory rather than in a ROM. Flash BIOSs can be upgraded in place, whereas ROM BIOSs must be replaced with a newer chip.

Floating Point Unit (FPU): A device which can perform calculations on numbers in floating point format as opposed to simple integers.

I

IDE (Integrated Drive Electronics): A standard of signalling and communicating with a device.

interleave: Multiple banks of memory that overlap to reduce the access time and eliminate wait states.

interrupt: Temporarily halting the operation of a digital computer to respond to (service) an external event.

interval timer: A device that can generate a pulse at a defined interval for background tasks.

IRQ (Interrupt Request): A signal channel used to trigger the CPU to temporarily change tasks.

K

Kilobyte (KB): 1,024 bytes.

N

ns (nano seconds): 1 x 10^{-9} seconds. (There are one billion nanoseconds in one second.)

P

page mode: The ability to read a whole line (page) of memory to reduce access time.

parity: A way to detect corrupted data in DRAM.

parallel port: An eight-bit port usually used for connecting a printer.

PCI (Peripheral Component Interconnect): Local bus for PCs that provides a high-speed data path between the CPU and peripherals (video, disk, network, etc.). The PCI bus coexists in the PC with the ISA or EISA bus. ISA and EISA boards still plug into an ISA or EISA slot, while high-speed PCI controllers plug into a PCI slot. The PCI bus runs at 33MHz, supports 32-bit and 64-bit data paths and bus mastering. The first PCs with PCI buses became available toward the end of 1993.

port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

R

RAM (Random Access Memory): The memory used to execute applications while your computer is turned ON. When you turn your computer OFF, all data stored in RAM is lost.

real-time clock (RTC): A CMOS counter used to maintain local time.

retaining bracket: The bracket on the end of the board that attaches to the back of the chassis and contains connectors, usually key board, mouse, serial port, and/or parallel port.

Appendix 2 Glossary of Terms

S

serial port: A two channel port, one channel used for "In" transmissions and one for "Out" transmissions.

SCSI (Small Computer System Interface): A high speed, general purpose interface to storage devices.

SRAM (Static Random Access Memory): As opposed to DRAM, this memory does not need to be refreshed by a controller and holds its information as long as the power is on.

T

tag comparator: A memory that tells whether an address is available in the cache.

U

UART (Universal Asynchronous Receiver Transmitter): A circuit that transmits and receives data on the serial port. It converts bytes into serial bits for transmission, and vice versa, and generates and strips the start and stop bits appended to each character.

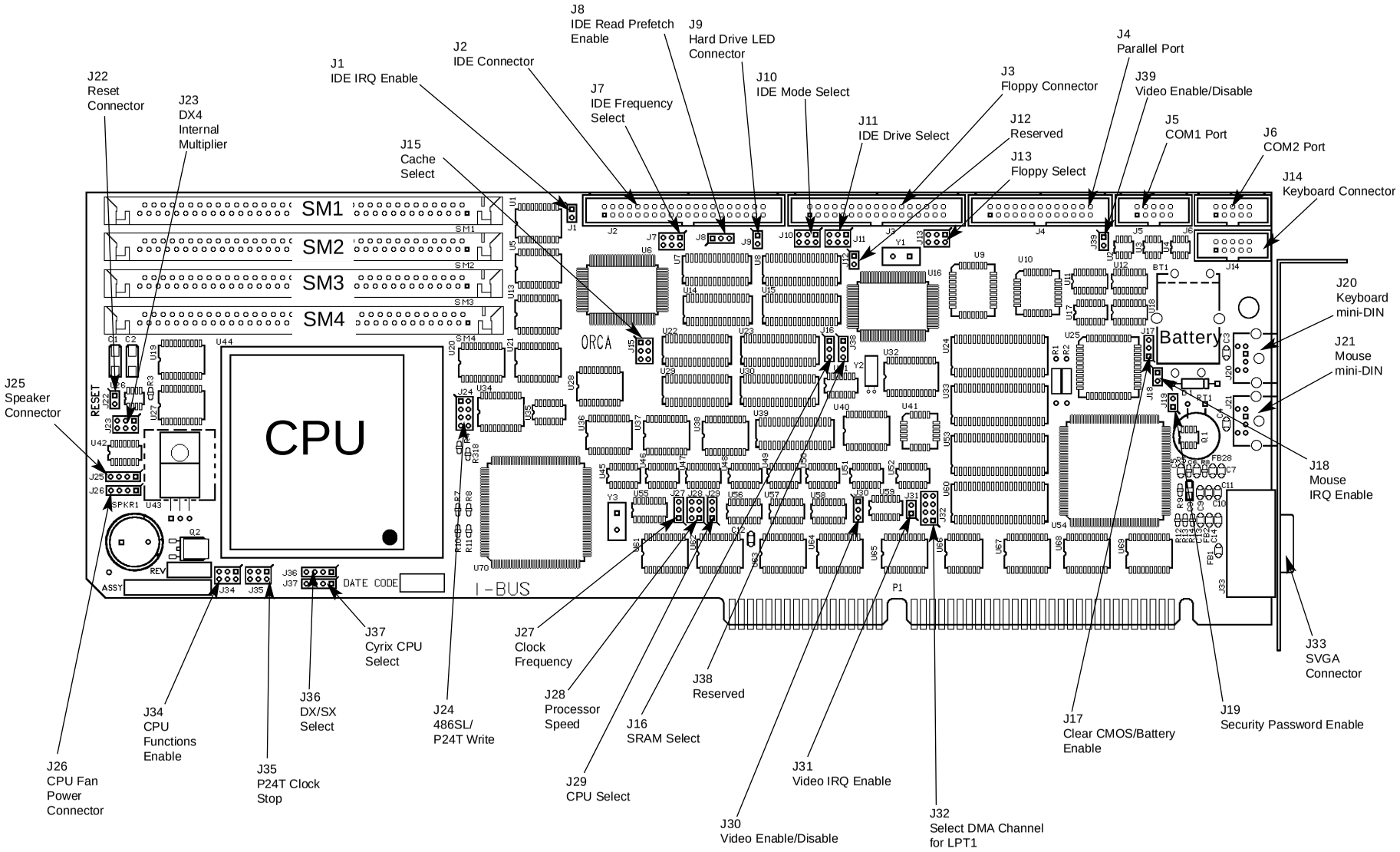
W

wait states: Extra time inserted to allow access to slower devices (e.g. DRAM) or EPROMS.

watchdog timer: A device that watches for CPU inactivity and then resets the CPU after a specified duration of inactivity.

write-back cache: The process where the CPU updates the cache and the DRAM simultaneously but does not wait for the DRAM to complete the update.

write-through cache: The process where the CPU updates the cache and the DRAM simultaneously but the CPU waits for the DRAM to complete the update, resulting in more time being consumed than in write-back.



ORCA Passive Backplane CPU Board

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