Table of Contents

Table of Contents

List of Tables (Continued)

Table of Contents

List of Figures

Chapter 1 Introduction

Welcome to the I-Bus family of passive backplane CPU (Central Processing Unit) boards. This manual contains information necessary to configure your CPU board to your specific needs.

The *Thresher™ CPU board* is IBM PC-AT compatible, utilizing the Pentium® Pro processor. It provides a passive backplane interface for both PCI and ISA expansion as well as providing conventional CPU board peripherals.

This chapter is divided into three sections:

- *About this manual*

  explains how this manual is laid out and what you can expect to find in it.

- *Preparing the board*

  describes the procedure for unpacking the Thresher CPU board and preparing it for use in your system.

- *Features of the board*

  provides a brief overview of the major components of the Thresher, accompanied by an illustration showing its jumpers, connectors, and components. For convenient reference, an illustration is provided at the back of this manual.

This manual contains four chapters pertaining specifically to your CPU board. The appendices contain technical reference material, a glossary of terms, and an illustration of the board, followed by an index.

- ### Chapter 1 Introduction

  introduces you to this manual and to the Thresher CPU board.

- ### Chapter 2 Jumpers and Connectors

  describes the jumpers and connectors on the Thresher CPU board. First, each jumper is described. A table shows where to place the jumper for your specific configuration. An illustration of the jumper indicates the pin numbers. Second, each connector is described. A table shows the pin-out descriptions and an illustration shows the pin numbers of each connector.

- ### Chapter 3 Specifications

  provides the component data and environmental characteristics of the Thresher CPU board.

- ### Chapter 4 BIOS

  explains how to use the BIOS setup utility firmware of the Thresher CPU board.

- ### Appendix 1 Technical Reference

  provides additional information to help you configure your CPU board and attach external peripheral devices. Included are I/O Maps, I/O Channels, Interrupt assignments, Address Maps, and ISA and PCI connector pin assignments.

- ### Appendix 2 Glossary of Terms

  contains definitions of terms used in this manual as well as terms that refer to items discussed.

- ### Appendix 3 Illustration

  provides a convenient illustration of the Thresher CPU board.

- *Index*

  provides easy access to page numbers of items discussed.

Preparing the board

• Unpacking your CPU board

The Thresher CPU board is shipped in a sealed, anti-static shielded bag.

- Open the bag at a static-free workstation while observing proper Electrostatic Discharge (ESD) practices.
- When not installed in a computer chassis, this board must be sealed in an ESD-approved shielded bag.
- This board must be shipped in a sealed, ESD-approved shielded bag and protected with anti-static packaging material (e.g., bubble wrap).
- I-Bus reserves the right to refuse warranty service on units not properly packaged to protect against ESD damage.

CAUTION!

Components on this board are sensitive to damage from Electrostatic Discharge (ESD). Handling of this board should ONLY be done by a properly trained technician in an approved ESD work area!

Packaged with your Thresher CPU board are:

- a *Thresher PCI/Pentium® Pro CPU Board User Manual*
- optional memory
- a keyboard adapter cable
- optional cables

If any of the items have been damaged in shipping, notify the transit company and initiate an insurance claim. If any items are missing, contact I-Bus. Refer to the *Limited Warranty* at the back of this manual for further instructions.

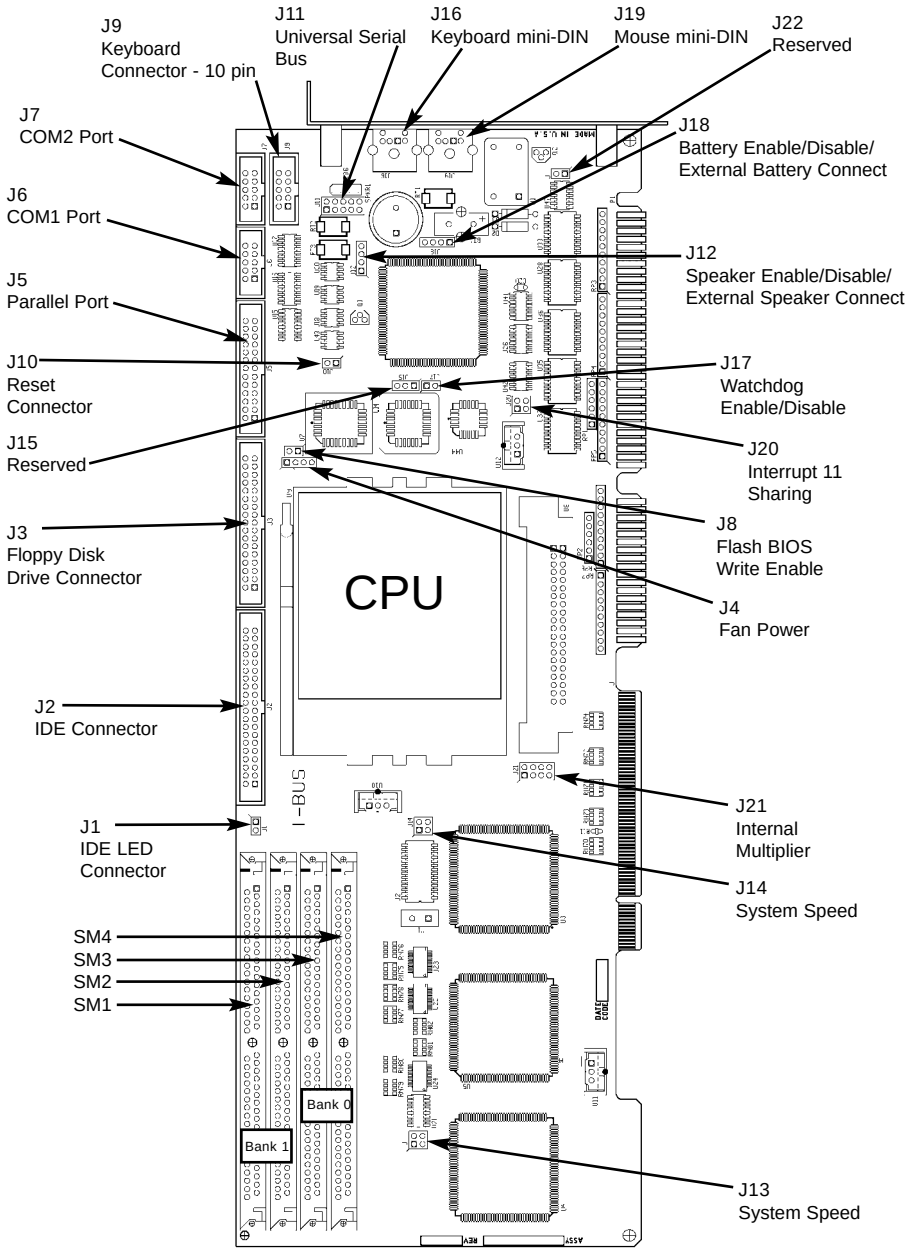


Figure 1-1: Thresher CPU Board Jumpers, Connectors and Components

Features

Some key features of the Thresher CPU board are:

- Pentium® Pro Central Processing Unit (CPU)
- Supports up to 512 MB of EDO, BEDO, FPM DRAM with Parity or ECC support
- Onboard floppy disk controller
- Two 16550-based serial ports and one bidirectional parallel port
- PCI Enhanced Integrated Drive Electronics (EIDE) hard disk interface
- PCI/ISA bridge
- Synchronous PCI interface
- Two-stage Watchdog timer

The following are detailed descriptions of the above features:

• Pentium® Pro CPU

- Pentium Pro bus protocol
- 64-bit Pentium Pro bus operating at 50.0 to 66.67MHz
- 36-bit address decode, 36-bit address drive
- 256KB or 512KB internal cache available
- Available at 180MHz and 200MHz core speeds
- Binary compatible with applications running on previous members of the Intel microprocessor family
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Dynamic Execution mircroarchitecture
- Single package includes Pentium Pro processor CPU, cache and system bus interface

- Separate dedicated external system bus and dedicated internal full-speed cache bus
- 8KB / 8KB separate data and instruction, non-blocking, level one cache
- Available with integrated 256KB or 512KB, non-blocking, level two cache on package
- Data integrity and reliability features include ECC, Fault Analysis/Recovery, and Functional Redundancy Checking
- Upgradable to a Future OverDrive® processor

• DRAM

- 8 MB to 512 MB main memory
- 64/72-bit non-interleaved path to memory
- FPM (Fast Page Mode), EDO (Extended Data Out), BEDO (Extended Data Out-Burst Mode) DRAMS providing x-1-1-1 to x-4-4-4 burst capability
- Support for Auto Detection of Memory Type: BEDO, EDO, or FPM
- Support for 4, 16, and 64Mbit DRAM devices
- Support for Symmetrical and Asymmetrical DRAM addressing
- Configurable support for ECC or Parity
- ECC with single-bit Error Correction and multiple-bit Error Detection
- Read-around-write support for host and PCI DRAM read accesses

Total	BANK 0		BANK 1	
	SM3	SM4	SM1	SM2
8MB	4MB (1MB x 36)	4MB (1MB x 36)	--------	--------
16MB	8MB (2MB x 36)	8MB (2MB x 36)	--------	--------
32MB	16MB (4MB x 36)	16MB (4MB x 36)	--------	--------
64MB	32MB (8MB x 36)	32MB (8MB x 36)	--------	--------
128MB	64MB (16MB x 36)	64MB (16MB x 36)	--------	--------
256MB	128MB (32MB x 36)	128MB (32MB x 36)	--------	--------
16MB	4MB (1MB x 36)	4MB (1MB x 36)	4MB (1MB x 36)	4MB (1MB x 36)
24MB	4MB (1MB x 36)	4MB (1MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)
40MB	4MB (1MB x 36)	4MB (1MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
72MB	4MB (1MB x 36)	4MB (1MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
136MB	4MB (1MB x 36)	4MB (1MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)
32MB	8MB (2MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)	8MB (2MB x 36)
48MB	8MB (2MB x 36)	8MB (2MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
80MB	8MB (2MB x 36)	8MB (2MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
144MB	8MB (2MB x 36)	8MB (2MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)
64MB	16MB (4MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)	16MB (4MB x 36)
96MB	16MB (4MB x 36)	16MB (4MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
160MB	16MB (4MB x 36)	16MB (4MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)
128MB	32MB (8MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)	32MB (8MB x 36)
192MB	32MB (8MB x 36)	32MB (8MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)
256MB	64MB (16MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)	64MB (16MB x 36)
512MB	128MB (32 MBx 36)	128MB (32 MBx 36)	128MB (32 MBx 36)	128MB (32 MBx 36)

Table 1-1: DRAM Configurations

- *PCI Bus Interface*
  - Derived clock mode provides a 66.66MHz Pentium Pro to 33.33MHz PCI, or 60MHz Pentium Pro to 30MHz PCI.
  - PCI Rev. 2.1, 5V interface compliant
  - Greater than 100MBps data streaming for PCI to DRAM accesses enables Native Signal Processing (NSP) on systems designed with the P6 processor
  - Integrated arbiter with multi-transaction PCI arbitration accelerator hooks

- Four PCI bus masters are supported in addition to the Host and PCI-to-ISA bridge
- Delayed Transaction support
- PCI parity checking and generation support
- Supports concurrent P6 and PCI transactions to main memory
- Extensive P6-to-DRAM and PCI-to-DRAM write data buffering
- Write combining support for P6-to-PCI burst writes

• Controller / I/O Features

- Floppy disk controller

  Software compatible with the DP8477, the 765A and the N82077

  16-byte FIFO (First-In-First-Out, disabled by default)

  Burst and non-burst modes

  High performance internal analog data separator (no external filter components required)

  Low power CMOS with power-down mode

  Automatic media-sense support with full IBM TDR (tape drive register) implementation for PC-AT and PS/2 floppy drive types

- Keyboard controller

  8042AH and PC87911 software compatible

  8-bit microcomputer with 2K custom ROM and 256 bytes data RAM

  Asynchronous access to two data registers and one status register during normal operation

  Supports both interrupt and polling

- Real-time clock

  DS1287, MC146818 and PC87911 compatible

  242 bytes battery backed-up CMOS RAM in two banks

Selective lock mechanism locks any half of the RTC RAM

Calendar in days, day of the week, months, and years with automatic leap-year adjustment

Time-of-day in seconds, minutes and hours:
12 or 24 hour format

Three individually maskable interrupt event flags:
Periodic rates from 122 μs to 500
Time of-day alarm once per second to once per day

Double buffer time registers

- UARTs

  Software compatible with the PC16550A and NS16450

- Parallel port

  EPP, ECP compatible with ECP level 2 support

  Bi-directional data transfer under software or hardware control

  Includes protection circuit to prevent damage to the parallel port when a connected printer is powered up or is operated at a higher voltage

- Address decoder

  Provides selection of all primary and secondary ISA addresses including COM1 through COM4

- Plug and Play

  Flexible IRQs and DMAs to meet the Plug and Play requirements of Microsoft's *PC '95 Hardware Design Guide*

  Multi-programmable parallel port base address

• *PCI to ISA Bridge Features*

- 100% PCI and ISA Compatible

  PCI and ISA master/slave interface

  Directly drives 4 PCI slots and 19 ISA slots

Supports PCI from 25-33 MHz

Supports ISA from 7.5-8.33 MHz

- Fast IDE Interface

  Supports PIO and Bus Master IDE

  Supports up to Mode 4 timings

  8 x 32-bit buffer for bus master IDE PCI burst transfers

- Steerable PCI Interrupts for PCI Device Plug-n-Play
- PCI Specifications Revision 2.1 Compliant
- Integrates the Functionality of One 82C54 Timer

  System timer

  Refresh request

  Speaker tone output

- Two 82C59 Interrupt Controller Functions

  14 Interrupts supported

  Independently programmable for edge/level sensitivity

- Enhanced DMA Functions

  Compatible DMA transfers

  27-bit addressability

  Two 8237 DMA controllers

  Fast type FDMA

  Seven independently programmable channels

- Universal Serial Bus (USB) Host Controller

  Compatible with Universal Host Controller Interface (UHCI)

  Contains Root Hub with two USB ports

- Non-Maskable Interrupts (NMI)

  PCI system errors

  ISA parity errors (ISA IOCHK assertion)

- Integrated data buffers to improve performance

  8-byte DMA/ISA master line buffer

  32-bit posted memory write buffer to ISA

- Integrated 16-bit BIOS timer
- Four dedicated PCI interrupts

  Level sensitive

  Can be mapped to any unused interrupt

- Arbitration for ISA devices

  ISA masters

  DMA and refresh

- Arbitration for PCI devices

  Six PCI masters are supported

  Fixed, rotating, or a combination of the two

- Utility bus (X-BUS) peripheral support

  Provides chip select decodes

  Controls lower X-BUS data byte transceiver

- *Watchdog Timer*

The dual stage watchdog timer is enabled as follows:

First, a “1” must be written to I/O address 0x160. Once the watchdog timer is enabled, it will generate an IRQ11 after sixteen seconds. After another sixteen seconds the board will reset. To prevent these exceptions from being generated, the timer is required to be serviced. It is serviced by writing a “1” to 0x164. It is disabled by writing a “0” to I/O address 0x160

Chapter 2 Jumpers and Connectors

This chapter describes the jumpers and connectors on the Thresher CPU board. Jumpers and connectors are identified by the label shown beside them on the board (e.g. J1), followed by the description (e.g. IDE Connector). A table shows the jumper settings or connector pin-outs for each jumper and connector. Illustrations of jumpers and connectors are shown from the component side of the board. Pin 1 is identified by the black pin.

All of the jumpers and connectors are shown on the illustration on page 1-4, *Figure 1-1, Thresher CPU Board Jumpers, Connectors, and Components* and on the illustration on page A3-1.

Pin 1 can be identified on the solder side of the board by the square pad in a connector or jumper.

CAUTION!

Components on this board are sensitive to damage from Electrostatic Discharge (ESD). Handling of this board should ONLY be done by a properly trained technician in an approved ESD work area!

The following jumpers are factory-set. If the system is reconfigured, some of the jumpers may need to be reset.

Note: In the tables that follow, an asterisk indicates the factory-set, default position of the jumper.

Jumper	Description	No. of Pins
J8	Flash BIOS Write Enable	2
J12	Speaker Enable/Disable/ External Speaker Connect	4
J13	System Speed	4
J14	System Speed	4
J15	Reserved	3
J17	Watchdog Enable/Disable	2
J18	Battery Enable/Disable/ External Battery Connect	4
J20	Interrupt 11 Sharing	4
J21	Internal Multiplier	8
J22	Reserved	2

Table 2-1: Jumpers

• *J8, Flash BIOS Write Enable*

To update Flash BIOS, place a jumper on pins 1 and 2. Normally there should be no jumper on pins 1 and 2.

Position	Function
1 & 2	Enable write to Flash BIOS
* OFF	Disable write to Flash BIOS

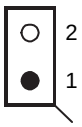


Table 2-2: J8, Flash BIOS Write Enable

- *J12, Speaker Enable/Disable/External Speaker Connect*

Placing a jumper on pins 1 and 2 enables the on-board speaker. If no jumper is placed on J12, the on-board speaker is disabled. An external speaker is connected to pins 1 (GND) and 4 (+).

Position	Function
*1 & 2	Enables on-board speaker
OFF	Disables on-board speaker
1 & 4	Connects external speaker

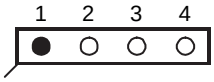


Table 2-3: J12, Speaker Enable/Disable/External Speaker Connect

- *J13, System Speed*

Use the following chart and the chart for jumper J21 to determine the proper jumper settings for the installed CPU. Please note that J13 and J14 must be configured with the same setting.

Jumpers		Speed
1 & 3	2 & 4	
OFF	ON	66 MHz
ON	OFF	60 MHz

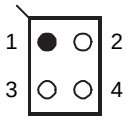


Table 2-4: J13, System Speed

• J14, System Speed

Use the following chart and the chart for jumper J21 to determine the proper jumper settings for the installed CPU. Please note that J13 and J14 must be configured with the same setting.

Jumpers		Speed
1 & 3	2 & 4	
OFF	ON	60 MHz
ON	OFF	66 MHz

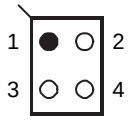


Table 2-5: J14, System Speed

• J21, Internal Multiplier

These jumper settings and the jumper settings listed for J13 and J14 are directly related to the installed CPU speed. Refer to the settings for J13 and J14 before making any changes to these jumpers.

Jumpers				Clock Ratio	J13 Settings	J14 Settings	Installed CPU Speed
1 & 2	3 & 4	5 & 6	7 & 8				
OFF	ON	ON	ON	2.5	60 MHz	60 MHz	150 MHz
OFF	ON	ON	ON	2.5	66 MHz	66 MHz	166 MHz
ON	ON	OFF	ON	3	60 MHz	60 MHz	180 MHz
ON	ON	OFF	ON	3	66 MHz	66 MHz	200 MHz

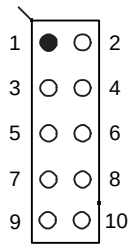


Table 2-6: J21, Internal Multiplier

• J15, Factory Reserved

- *J17, Watchdog Enable/Disable*

To enable the watchdog timer, place a jumper on pins 1 and 2. The address of the watchdog timer is I/O 160 and cannot be relocated. To free I/O 160 for use with other devices, the watchdog timer must be disabled. To disable the watchdog timer, remove the jumper from J17.

Position	Function
1 & 2	Watchdog Enabled
*OFF	Watchdog Disabled

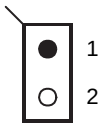


Table 2-7: J17, Watchdog Enable/Disable

- *J18, Battery Enable/Disable/External Battery Connect*

Placing a jumper on pins 1 and 2 enables the on-board battery. If no jumper is placed on J18, the on-board battery is disabled. An external battery is connected to pins 1 (+) and 4 (GND).

Position	Function
* 1 & 2	Enables on-board battery
OFF	Disables on-board battery
1 (+) & 4 (GND)	Connects external battery

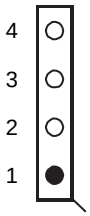


Table 2-8: J18, Battery Enable/Disable/External Battery Connect

- *J20, Interrupt 11 Sharing*

Placing a jumper on pins 3 and 4 makes IRQ11 available to the ISA bus. Placing jumpers on pins 1 & 3 and 2 & 4 allows IRQ11 to be shared with the watchdog timer. Placing a jumper on pins 1 and 3 makes IRQ11 available for the watchdog timer only. If no jumper is placed on J20, IRQ11 is not available.

Position	Function
* 3 & 4	IRQ11 pullup to ISA bus (default)
1 & 3, 2 & 4	IRQ11 shared with watchdog timer
1 & 3	IRQ11 used by watchdog timer
None	IRQ11 not available

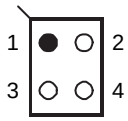


Table 2-9: J20, Interrupt 11 Sharing

- *J22, Factory Reserved*

Connectors

The following connectors can be located in *Figure 1-1: Thresher CPU Board Jumpers, Connectors, and Components* on page 1-4, and the fold-out illustration on page A3-1.

Jumper	Description	No. of Pins
J1	Hard Drive LED Connector	2
J2	IDE Connector	40
J3	Floppy Disk Drive Connector	34
J4	CPU Fan Power	4
J5	Parallel Port	26
J6	COM1 Port	10
J7	COM2 Port	10
J9	Keyboard Connector - 10 pin	10
J10	Reset Connector	2
J11	Universal Serial Bus	10
J16	Keyboard mini-DIN	6
J19	Mouse mini-DIN	6

Table 2-10: Connectors

- ### J1, Hard Drive LED Connector

Installing the Hard Drive LED connector on J1 lights the LED on the front panel when the IDE drive is active.

Pin #	Name
1	Cathode
2	Anode

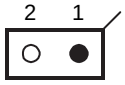
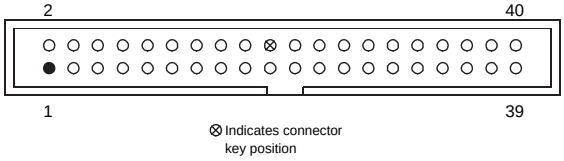


Table 2-11: J1, Hard Drive LED Connector

- *J2, IDE Connector*

Pin #	Name	Pin #	Name
1	$\overline{\text{RST}}$	21	N/C
2	GND	22	GND
3	D7	23	IOW
4	D8	24	GND
5	D6	25	IOR
6	D9	26	GND
7	D5	27	N/C
8	D10	28	CBLSEL
9	D4	29	N/C
10	D11	30	GND
11	D3	31	IRQ14
12	D12	32	IO16
13	D2	33	SAI
14	D13	34	N/C
15	D1	35	SA0
16	D14	36	SA2
17	D0	37	CS0
18	D15	38	CS1
19	GND	39	HDIND
20	Key	40	N/C

Table 2-12: J2, IDE Connector

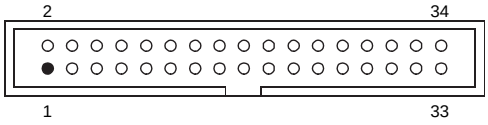


- *J3, Floppy Disk Drive Connector*

Pin #	Name
2	RPM/LC
4	N/C
6	ID0
8	$\overline{\text{INDEX}}$
10	$\overline{\text{MTRO}}$
12	$\overline{\text{DRV1}}$
14	$\overline{\text{DRV0}}$
16	$\overline{\text{MTR1}}$
18	DIR
20	$\overline{\text{STEP}}$
22	$\overline{\text{WDATA}}$
24	$\overline{\text{WGATE}}$
26	$\overline{\text{TRK0}}$
28	$\overline{\text{WPRT}}$
29	ID0
30	$\overline{\text{RDATA}}$
32	HDSEL
33	ID1
34	DSKCHG
*	GND

Table 2-13: J3, Floppy Connector

* The remainder of the odd numbered pins are GND.



- *J4, CPU Fan Power*

To connect a CPU fan to the board, install a 4-pin connector on J4.

Pin #	Name
1	+12V
2	N/C
3	N/C
4	GND

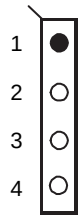


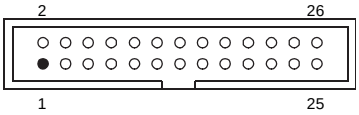
Table 2-14: J4, CPU Fan Power

- *J5, Parallel Port*

J5 is a 26-pin shrouded header for the parallel port interface.

Pin #	Name	Pin #	Name
1	$\overline{\text{Strobe}}$	2	AutoFeed
3	+ Data bit 0	4	Error
5	+ Data bit 1	6	Init
7	+ Data bit 2	8	SLCT IN
9	+ Data bit 3	10	GND
11	+ Data bit 4	12	GND
13	+ Data bit 5	14	GND
15	+ Data bit 6	16	GND
17	+ Data bit 7	18	GND
19	ACK	20	GND
21	Busy	22	GND
23	Paper Empty	24	GND
25	GND	26	N/C

Table 2-15: J5, Parallel Port



• J6, COM1 Port

The primary serial port is a ten-pin header located at J6. The primary serial port can be terminated in a DB9 connector by obtaining the optional serial port cable from I-Bus. A wire list is also provided on page 2-14 for a third-party cable.

Another optional cable from I-Bus is equipped with a retaining bracket mounting a DB9 and a DB25 connector terminating in a ten-pin and twenty-six pin header, respectively. See Table 2-18 for DB9 and DB25 wiring information.

Pin #	Name
1	$\overline{\text{DCD}}$
2	$\overline{\text{DSR}}$
3	RXD
4	$\overline{\text{RTS}}$
5	TXD
6	$\overline{\text{CTS}}$
7	$\overline{\text{DTR}}$
8	$\overline{\text{RI}}$
9	GND
10	N/C

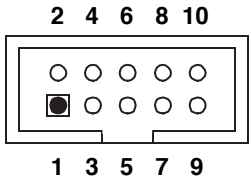


Table 2-16: J6, COM1 Port

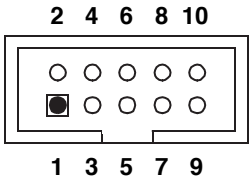
- *J7, COM2 Port*

The secondary serial port is a ten-pin header located at J7. The secondary serial port can be terminated in a DB9 connector by obtaining the optional serial port cable from I-Bus. A wire list is also provided on page 2-14 for a third-party cable.

Another optional cable from I-Bus is equipped with a retaining bracket mounting a DB9 and a DB25 connector terminating in a ten-pin and twenty-six pin header, respectively. See Table 2-18 for DB9 andDB25 wiring information.

Pin #	Name
1	$\overline{\text{DCD}}$
2	$\overline{\text{DSR}}$
3	RXD
4	$\overline{\text{RTS}}$
5	TXD
6	$\overline{\text{CTS}}$
7	$\overline{\text{DTR}}$
8	$\overline{\text{RI}}$
9	GND
10	N/C

Table 2-17: J7, COM2 Port

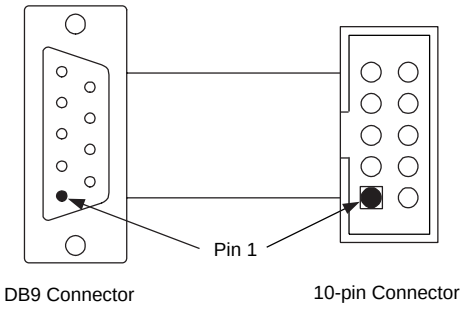


• Serial Port Cable Wire List

The following wire list is provided for users who want to make a cable that connects to a serial port connector and terminates with either a DB9 (shown) or DB25 (RS232) connector.

Signal Name	Connector		
	Onboard 10 Pin Connector (J4 or J6)	25 Pin	9 Pin
$\overline{\text{DCD}}$	1	8	1
$\overline{\text{DSR}}$	2	6	6
RXD	3	3	2
$\overline{\text{RTS}}$	4	4	7
TXD	5	2	3
$\overline{\text{CTS}}$	6	5	8
$\overline{\text{DTR}}$	7	20	4
$\overline{\text{RI}}$	8	22	9
GND	9	2	5
N/C	10	N/C	N/C

Table 2-18: Serial Port Cable Wire List



Pin #	Name
1	CLOCK
2	GND
3	DATA
4	N/C
5	N/C
6	N/C
7	+5 V
8	Key
9	N/C
10	GND

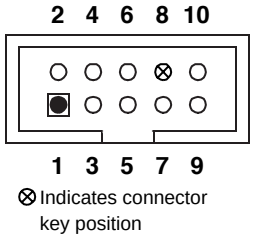


Table 2-19: J9, Keyboard Connector - 10-pin

• *J9, Keyboard Connector - 10 pin*

J9 accepts a 10-pin keyboard connector.

Pin #	Name
1	Reset
2	Ground

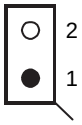


Table 2-20: J10, Reset Connector

• *J10, Reset Connector*

An external reset cable can be attached to the Thresher at J1. Momentarily shorting Pin 1 (Reset) to Pin 2 (GND) while the CPU board is operating will activate the Reset function.

- *J11, Universal Serial Bus*

The Universal Serial Bus (USB) allows for the connection of up to 127 USB-supported peripherals.

Pin #	Name
1	+5V
2	+5V
3	Port0-
4	Port1-
5	Port0+
6	Port1+
7	Port0 GND
8	Port1 GND
9	Port0 GND
10	Port1 GND

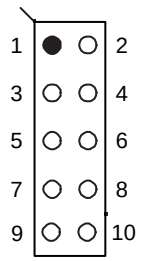


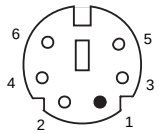
Table 2-21: J11, Universal Serial Bus

- *J16, Keyboard mini-DIN*

J16 is a six-pin mini-DIN keyboard connector located on the retaining bracket. A standard PC-AT compatible keyboard can also be used when fitted with the keyboard adapter cable furnished with the CPU board.

Pin #	Name
1	DATA
2	N/C
3	GND
4	+5 V
5	CLOCK
6	N/C

Table 2-22: J16, Keyboard mini-DIN



View from end of board

CAUTION!

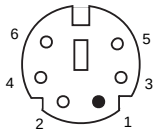
The mouse and keyboard mini-DIN connectors are identical. Make sure the correct accessory is plugged into its proper connector.

• J19, Mouse mini-DIN

J19 is a six-pin mini-DIN mouse connector located on the retaining bracket.

Pin #	Name
1	DATA
2	N/C
3	GND
4	+5 V
5	CLOCK
6	N/C

Table 2-23: J19, Mouse mini-DIN



View from end of board

CAUTION!

The mouse and keyboard mini-DIN connectors are identical. Make sure the correct accessory is plugged into its proper connector.

System Components

CPU:	Pentium® Pro CPU
Form Factor:	Standard full length AT
Interrupts:	15 levels available
Power Requirements:	Input Power +5 V @ 8 A with 16MB memory +12 V @ 120 mA -12 V @ 50 mA
Cache:	Internal to CPU
DRAM:	Supports up to 512MB of on-board and FPM, EDO, BEDO DRAM SIMM
System ROM:	Contains system Flash-BIOS
Clock/Calendar:	Real-time clock backed by an on-board lithium battery
External Connections:	EIDE & floppy (shrouded headers) USB (Universal Serial Bus) Bidirectional parallel port Serial port 1 (shrouded header) Serial port 2 (shrouded header) Keyboard (mini-DIN on retaining bracket) Mouse (mini-DIN on retaining bracket) Keyboard (ten-pin header) Speaker (header) Reset (header) Hard Drive LED (header)

Environmental	Operating	Non-operating
Temperature	0° to +55°C	-40° to +65°C
Humidity	5 to 95% @ 40°C non-condensing	5 to 95% @ 40°C non-condensing
Shock	2.5 g @ 10 ms	10 g @ 10 ms
Vibration	0.25 g @ 5-100 Hz	5 g @ 5-100 Hz

Table 3-1: Environmental Specifications

The BIOS Setup Utility allows you to configure your CPU board to your system. The BIOS, or Basic Input/Output System, is the on-board firmware that communicates with the display, keyboard, printers and other peripheral devices.

Starting and Exiting the BIOS Setup

When you turn on your computer, a test is conducted called the Power On Self Test, or POST. During this test the system checks for certain hardware configurations and compares them to the BIOS Setup Utility. If, at boot, the system status does not match the system configuration stored in CMOS, you will be prompted to start the BIOS Setup Utility.

To Start the BIOS Setup:

- During a cold boot, press <Del> when prompted.

To Exit the BIOS Setup and boot the computer:

- While in any utility screen, press <Esc> to return to the CMOS Setup Utility Screen. If SAVE & EXIT SETUP is selected, all configuration changes edited in the various screens are recorded in CMOS memory at this time. If EXIT WITHOUT SAVING is selected, if power is turned off, or if the front-panel reset button is pressed, the changes made in the BIOS will not be saved and the original configuration will remain unchanged.

- *All BIOS screens contain:*
  - a **body** consisting of the **entry fields** containing the utility's parameters.
  - a **bottom line** indicating the keystrokes that you can use to manipulate the cursor in that screen.

- *Manipulating the screens*

The arrow keys are used to highlight items. **Enter** is used to select, the **PageUp** and **PageDown** keys are used to change entries, **F1** is pressed for help, and **Esc** is pressed to quit.

- **<Up arrow>** Move to previous item
  <Down arrow> Move to next item
  <Left arrow> Move to the item on the left
  <Right arrow> Move to the item on the right
- **Esc** key - CMOS Setup Utility Screen - Quit and do not save changes into CMOS. All other screens, return to CMOS Setup Utility Screen.
- **PgUp** key - Increase the numeric value or make changes.
  PgDn key - Decrease the numeric value or make changes.
- **+** key - Increase the numeric value or make changes.
  - key - Decrease the numeric value or make changes.
- **F1** key - General help - Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit, press Esc or the F1 key again.
- **F2** key - Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward.
- **F3** key - Calendar, only for Standard CMOS Setup Screen.
- **F5** key - Restore the previous CMOS value from CMOS, only for BIOS Features Setup Screen.
- **F6** key - Load the default CMOS value from BIOS default table, only for BIOS Features Setup Screen.
- **F7** key - Load Setup defaults.
- **F10** key - Save all CMOS changes, only for CMOS Setup Utility Screen.

This section describes each setup screen in the CMOS Setup Utility.

Screens and Commands identified on the CMOS Setup Utility Menu are:

- Standard CMOS Setup
- BIOS Features Setup
- Chipset Features Setup
- Power Management Setup
- PNP/PCI Configuration
- Load BIOS Defaults
- Load Setup Defaults
- Integrated Peripherals
- Supervisor Password
- User Password
- IDE HDD Auto Detection
- HDD Low Level Format
- Save & Exit Setup
- Exit Without Saving

In this section each utility is represented by:

- Screen Illustration
- Explanation
- Entry Fields

Screen Illustration

The screens presented in this manual reflect the same format as your screens. However, entry values and selections shown on these screens are ***examples only.***

Explanation

The explanation following each screen illustration describes the utility and the available choices.

Entry Fields

Each entry field in the body of the screen is described and all available choices, or parameters, are listed.

• *CMOS Override*

If the system fails to boot after changes are made to the BIOS Setup, a CMOS override can be invoked by pressing the **Insert** key when the computer is rebooted. This resets the system to its defaults. The system can be restarted by power-cycling the computer (turning the power switch OFF and then ON), by pressing the **RESET** button, or by pressing **Ctrl**, **Alt** and **Delete**.

• CMOS Setup Utility Screen

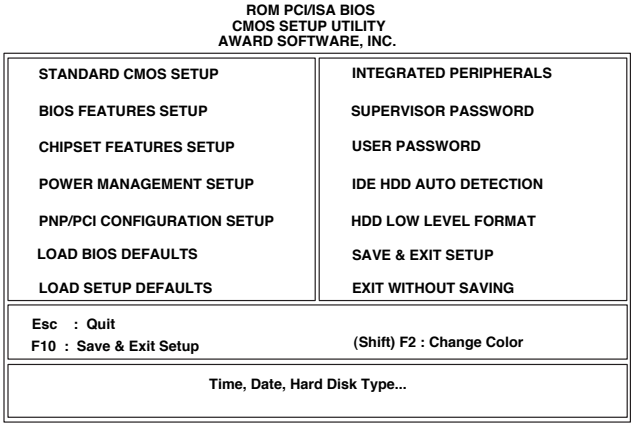


Figure 4-1: CMOS Setup Utility Screen

Explanation

The CMOS Setup Utility screen allows selection of eight setup screens and two exit choices. Use the arrow keys to move between choices and press **Enter** to select the highlighted choice.

Entry Fields

Standard CMOS Setup

This setup screen allows you to configure the calendar, hard drives, floppy drives, video mode and the “Halt On” command.

BIOS Features Setup

This setup screen allows you to configure virus warning, cache, boot sequence, keyboard, security, shadowing.

Chipset Features Setup

This setup screen allows you to configure the system memory and chipset specific items.

Power Management Setup

This setup screen only displays if the system supports Power Management (Green PC) standards.

PNP/PCI Configuration

This setup screen sets interrupts for PCI.

Load BIOS Defaults

This screen allows you to load the BIOS defaults for minimum system performance.

Load Setup Defaults

This screen allows you to load the chipset defaults for maximum system performance.

Integrated Peripherals

This screen allows configuration of system board peripherals.

Supervisor Password

This selection allows a supervisor to configure the change, set, or disable functions of the supervisor password option.

User Password

This selection allows you to configure the change, set, or disable functions of the user password option.

IDE HDD Auto Detection

Functions on this screen automatically detect and configure the hard disk parameters.

HDD Low Level Format

Functions on this screen allow you to perform a low-level format to a new hard drive.

Save & Exit Setup

Save CMOS changes and exit setup.

Exit Without Saving

Abandon all CMOS value changes and exit setup.

• Standard CMOS Setup Screen

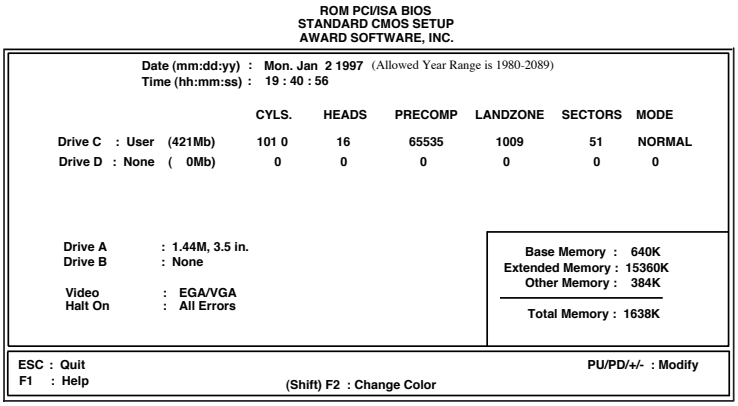


Figure 4-2: Standard CMOS Setup Screen

Explanation

The parameters in the Standard CMOS Setup Screen are divided into groups. Each group includes one or more setup items. Use the arrow keys to highlight the item and then use the **PgUp** or **PgDn** keys to select the value for each item.

Date. The month is highlighted first, then the date and year. Day is automatically calculated when the month and year are entered.

Hard Disks. identify the hard disk drives installed on the system. When numbers 1 to 45 are selected, the drive parameters are automatically configured. When "User" is selected, the drive parameters must be entered directly from the keyboard. When "Auto" is selected, the hard drive parameters will be automatically detected whenever the system is booted. Press **Enter** when the entry is complete.

Drives A/B. A: and B: identify the types of floppy disk drives installed on the system.

Video. This selection pertains to the primary system monitor. Secondary system monitors are supported but do not have to be selected in Setup.

Halt On. After boot up and during POST (Power On Self Test), the system will stop when it encounters an error or device not present. Select the way the system will boot up.

Memory. The memory is auto-sensed during POST. **No user entry is allowed.** Base Memory is the amount of memory at or about the 64KB boundary. Extended Memory is above the 1MB boundary. Other Memory is the portion of memory, usually 384K, allocated for Shadow RAM or remapped to the Extended Memory pool.

Entry Fields

Fields	Description	Choices
Date	*Sets the date. The format is day, month, year.*	*1. Jan-Dec* *2. 1-31* *3. 1980-2079*
Time	*Sets the time. The format is hour, minute, second on a 24-hour clock.*	*1. 1-24* *2. 1-60* *3. 1-60*
Drive C/Drive D	*Selects the hard drive parameter.*	*1. Auto* *2. 1-45* *3. None* *4. User (BIOS & Setup default)*

Table 4-1: Standard CMOS Setup Screen Entry Fields

Fields	Description	Choices
Drive A *Drive B*	*Selects the floppy drive unit installed.*	*1. None (BIOS & Setup default, drive B)* *2. 360K, 5.25in.* *3. 1.2M, 5.25 in.* *4. 720K, 3.5 in.* *5. 1.44M, 3.5 in. (BIOS & Setup default, drive A)* *6. 2.88M, 3.5 in.*
Video	*Select the type of video adapter used for the primary system monitor.*	*1. EGA/VGA (BIOS & Setup default)* *2. CGA 40* *3. CGA 80* *4. MONO*
Halt On	*Select the condition that would cause the system to stop at boot up.*	*1. All Errors (BIOS & Setup default)* *2. No Errors* *3. All, But Keyboard* *4. All, But Diskette* *5. All, But Disk/Key*

Table 4-1: Standard CMOS Setup Screen Entry Fields Cont'd

- *BIOS Features Setup Screen*

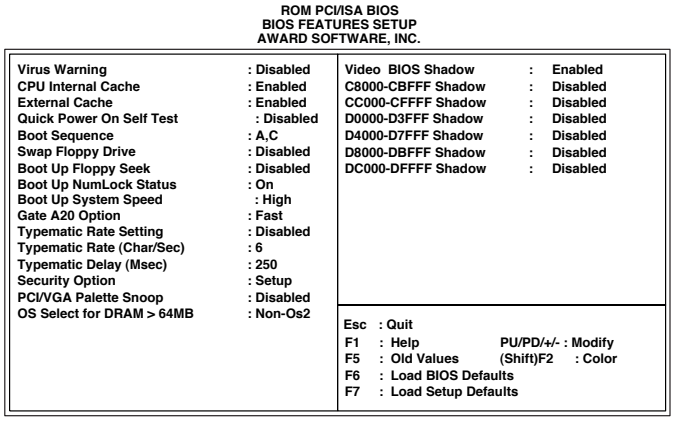


Figure 4-3: BIOS Features Setup Screen

Explanation

This setup screen contains parameters that configure the system for basic operation. Use the arrow keys to highlight the item and then use the **PgUp** or **PgDn** keys to select the value for each item.

Virus Warning. You will need to disable this option while using certain fixed disk maintenance programs (e.g., DOS FDISK), because their actions would be interpreted as a violation.

Boot Sequence. The BIOS assumes that Drive C is the hard disk drive and Drive A is the floppy disk drive.

Memory Parity/ECC Check. During system boot, the BIOS sizes and tests all memory. If an error is detected, an error message is displayed and the boot process is terminated. Disabling this feature bypasses the test and allows the system to boot.

Security Option. To disable the Security Option, select PASSWORD SETTING from the CMOS Setup Utility screen. When prompted to enter a new password, do not enter anything, just press **Enter**. This disables security. Once security is disabled, the system will boot and Setup can be entered.

Shadow RAM. Shadow RAM is a mechanism that copies Read Only Memory into main memory, then substitutes that memory image for the original ROM. This increases the execution speed of programming that resides in ROM. BIOS and VGA Adapters are two main examples of

ROMs that demonstrate significant performance gains when they are shadowed.

Since ROMs are by definition Read-Only, it is usually desirable to write protect the Shadow RAM. However, Shadow RAM can also be used as general purpose memory by certain programs. In this case, it should be enabled as Read-Write memory. While most Adapter ROMs can be shadowed either way, some permit only the RW or WP option, and a rare few cannot be shadowed at all. You may need to experiment a little.

Shadow RAM is obtained from a gap in the otherwise contiguous memory space of the computer. The 384K region between the 640K and 1MB boundaries is occupied not by memory, but instead by ROMs, video memory, and possibly other system-level devices. The memory that should appear there is simply inaccessible and unused. One way to make use of this lost memory is to activate it as Shadow RAM. Certain designs can also remap a portion of this 384K into the Extended Memory pool, provided it is not already enabled as Shadow RAM. In most designs with this capability, remap will be prevented if any Shadow segment is enabled in the D000 through E000 regions.

Entry Fields

Fields	Description	Choices
Virus Warning	*Enable to activate automatically when system boots, causing message to display.*	*1. Enabled* *2. Disabled (BIOS & Setup default)*
CPU Internal/ External Cache	*Enable to allow access to CPU internal and external cache.*	*1. Enabled (BIOS & Setup default)* *2. Disabled*
Quick Power On Self Test	*Speeds up Power On Self Test (POST) when enabled by skipping some of the tests.*	*1. Disabled (Setup default)* *2. Enabled (BIOS default)*
Boot Sequence	*Enter the drive sequence used to boot the system.*	*1. A,C (BIOS & Setup default).* *2. C,A* *3. C,CDROM,A* *4. CDROM,C,A*

Table 4-2: BIOS Features Setup Screen Entry Fields

Fields	Description	Choices
Swap Floppy Drive	*Enable to reassign floppy drive designation if more than one floppy drive is installed in the system.*	*1. Disabled (BIOS & Setup default)* *2. Enabled*
Boot Up Floppy Seek	*During POST, the BIOS determines if the installed floppy drive is 40 or 80 tracks. 360K type is 40 tracks. 720K, 1.2M, and 1.44M are all 80 tracks.*	*1. Disabled (BIOS default)* *2. Enabled (Setup default)*
Boot Up NumLock Status	*Enter the default state of the numeric keypad at boot up.*	*1. Off* *2. On (BIOS & Setup default).*
Boot Up System Speed	*"High" selects the normal system operating speed during system boot.*	*1. Low* *2. High (BIOS & Setup default).*
Gate A20 Option	*"Normal" handles A20 gate through the keyboard. Fast handles A20 gate through the chipset.*	*1. Normal (BIOS default)* *2. Fast (Setup default)*
Typematic Rate Setting	*Enable to allow a key to repeat when pressed. Disable to keep a key from repeating when it is pressed.*	*1. Disabled (BIOS & Setup default).* *2. Enabled*
Typematic Rate (Chars/Sec)	*Enter the rate at which a key repeats when pressed. (Typematic Rate Setting must be enabled.)*	*1. 6 (BIOS & Setup default)* *8, 10, 12, 15, 20, 24, 30*

Table 4-2: BIOS Features Setup Screen Entry Fields Cont'd

Fields	Description	Choices
Typematic Delay (Msec)	Enter the length of time a key can be pressed before it will begin to repeat. (Typematic Rate Setting must be enabled.)	1. 250 (BIOS & Setup default) 2. 500 3. 750 4. 1000
Security Option	Enter "System" to require password to access system. Enter "Setup" to require password to enter setup.	1. Setup (BIOS & Setup default). 2. System
PCI/VGA Palette Snoop	Enable the VGA feature connector port.	1. Disabled (BIOS & Setup default). 2. Enabled
OS Select For DRAM > 64MB	Enter "OS2" if the system is running the OS2 operating system and more than 64MB of DRAM is installed.	1. Non-OS2 (BIOS & Setup default). 2. OS2
Video BIOS Shadow	Enabling video shadow copies video shadow to RAM, increasing video speed.	1. Disabled 2. Enabled (BIOS & Setup default).
C8000-CBFFF/ DC000-DFFFF Shadow	Enable optional ROM to RAM in each of the defined areas.	1. Disabled (BIOS & Setup default). 2. Enabled

Table 4-2: BIOS Features Setup Screen Entry Fields Cont’d

- *Chipset Features Setup Screen*

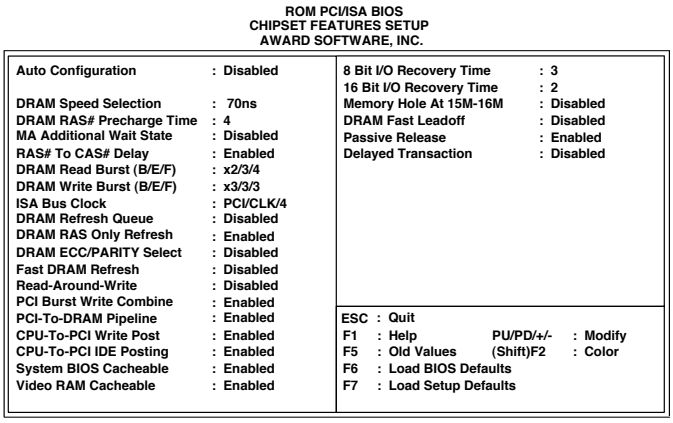


Figure 4-4: Chipset Features Setup Screen

Explanation

The Chipset Features Setup screen manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. Normally, these items never need to be altered. The setup default settings provide optimum conditions for the system. The only time changes are warranted is if data is being lost during system use.

CPU Read Multiple Prefetch. A prefetch occurs during a process (eg., reading from the PCI or memory) when the chipset "peeks" at the next instruction and actually begins the next read instruction. The chipset has four read lines. A multiple prefetch means that the chipset has the capacity to initiate more than one prefetch during a process.

CPU Line Read Multiple. A line read means that the CPU is reading a full cache line. When a cache line is full it holds 32 bytes of data. Because the line is full, the system knows exactly how much data it will be reading and it doesn't need to wait for an end-of-data signal, freeing it to do other things. When enabled, the system is allowed to read more than one full cache line at a time.

DRAM Settings. DRAM refresh takes place as two pulses of power, one for the columns of data (called Column Address Strobe or CAS) and one for the rows (Row Address Strobe or RAS). The CAS and RAS are also employed when reading and writing data to DRAM.

8 & 16 Bit I/O Recovery Time. The recovery time is the length of time, in CPU clocks, the system will delay after the completion of an input/output request. This delay is required because the CPU is operating faster than the I/O bus. Therefore, the CPU must be delayed to allow for completion of the I/O.

Entry Fields

Fields	Description	Choices
Auto Configuration	*Enabling Auto Configuration selects predetermined, optimal chipset parameter values. Disabling reverts chipset parameters to setup information stored in CMOS.*	*1. Disabled* *2. Enabled (BIOS & Setup default).*
DRAM Speed Selection	*Set to the type of DRAM SIMMs installed in the system.*	*1. 70 (BIOS & Setup default).* *2. 60*
DRAM RAS# Precharge Time	*Selects the number of cycles for RAS (Row Address Strobe) to charge before DRAM refresh. 3 gives faster performance, 4 gives more stable performance. This field can only be changed when Auto Configuration is set to "disabled."*	*1. 3* *2. 4 (BIOS & Setup default).*
MA Additional Wait State	*Enabling inserts an additional wait state before the beginning of a memory read. This field can only be changed when Auto Configuration is set to "sidabled."*	*1. Disabled (Setup default)* *2. Enabled (BIOS default).*
RAS# to CAS# Delay	*Rows and columns are addressed separately when DRAM is refreshed. Enable inserts a delay between the CAS and RAS strobe signals. Disabled is faster. Enabled is more stable. This field can only be changed when Auto Configuration is set to "disabled."*	*1. Disabled* *2. Enabled (BIOS & Setup default).*
DRAM Read Burst (B/E/F)	*Sets the timing for bust-mode reads from DRAM. The lower the timing numbers, the faster the system addresses memory. This field can only be changed when Auto Configufation is set to "disabled."*	*1. x3/4/4* *2. x2/3/4 (BIOS & Setup default)* *3. x2/2/3* *4. x1/2/3*

Table 4-3: Chipset Features Setup Screen Entry Fields

Fields	Description	Choices
DRAM Write Burst (B/E/F)	*Set the timing for burst-mode writes from DRAM. The lower the timing numbers, the faster the system addresses memory. This field can only be changed if Auto Configuration is set to "disabled."*	*1. x4/4/4* *2. x3/3/4* *3. x3/3/3 (BIOS & Setup default)* *4. x2/2/3*
ISA Bus Clock	*Selects the speed of the ISA bus based on the speed of the PCI bus. If the PCI bus is operating at 33MHz, PCI CLK/4 yields an ISA bus speed of approximately 8MHz, the standard speed of the ISA bus. This field can only be changed if Auto Configuration is set to "disabled."*	*1. PCI CLK/4 (BIOS & Setup default)* *2. PCI CLK/3*
DRAM Refresh Queue	*Enabling permits queuing up to 4 DRAM refresh requests allowing DRAM to refresh at optimal times. Disabling makes all refreshes priority requests.*	*1. Disabled (BIOS default)* *2. Enabled (Setup default)*
DRAM RAS only Refresh	*Enables the chipset to perform a read in order to refresh.*	*1. Enabled (BIOS & Setup default)* *2. Disabled*
DRAM ECC/ PARITY Select	*Select Disabled, Parity, or ECC depending on the type of installed DRAM.*	*1. Disabled (Setup default)* *2. Parity (BIOS default)* *3. ECC*
Fast DRAM Refresh	*Enabling permits CAS strobe to be in the "hidden" mode, increasing refresh speed.*	*1. Disabled (BIOS & Setup default).* *2. Enabled*
Read-Around-Write	*Enable allows reads to bypass writes as long as reads and writes are not accessing the same address. DRAM optimization feature*	*1. Disabled (BIOS default)* *2. Enabled (Setup default)*

Table 4-3: Chipset Features Setup Screen Entry Fields Cont'd

Fields	Description	Choices
PCI Burst Write Combine	*Enable allows the chipset to assemble long PCI bursts from the data held in the PCI buffers.*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
PCI-To-DRAM Pipeline	*Enable allows full PCI-to-DRAM write pipelining. DRAM optimization feature.*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
CPU-To-PCI Write Post	*Enable allows writes from the CPU to the PCI bus to be buffered.*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
CPU-To-PCI IDE Posting	*Enable posts write cycles from the CPU to the PCI IDE interface. IDE accesses are posted in the CPU to PCI buffers for cycle optimization.*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
System BIOS Cacheable	*Enabling allows accesses to the system BIOS ROM addressed at F0000H-FFFFFH to be cached, provided that the cache controller is enabled.*	*1. Disabled (Setup default)* *2. Enabled (BIOS default)*
Video RAM Cacaheable	*Enabling allows access to the video BIOS ROM addressed at C0000H-C7FFFH to be cached, provided that the cache controller is enabled.*	*1. Disabled (Setup default)* *2. Enabled (BIOS default)*
8 Bit I/O Recovery Time	*The length of time, in CPU clocks, to delay the CPU after the completion of an 8-bit I/O request. This selection is used to compensate for the difference in speed between the CPU and the I/O bus.*	*1. N/A* *2. 8* *3. 1 (Setup default)* *4. 2* *5. 3 (BIOS default)* *6. 4* *7. 5* *8. 6* *9. 7*

Table 4-3: Chipset Features Setup Screen Entry Fields Cont'd

Fields	Description	Choices
16 Bit I/O Recovery Time	*The length of time, in CPU clocks, to delay the CPU after the completion of a 16-bit I/O request. This selection is to compensate for the difference in speed between the CPU and the I/O bus.*	*1. NA 2. 4 3. 1 (Setup default). 4. 2 (BIOS default). 5. 3*
Memory Hole At 15M-16M	*Enabling reserves this area of system memory for the ISA adapter ROM.*	*1. Disabled (BIOS & Setup default). 2. Enabled*
DRAM Fast Leadoff	*Enabling shortens the leadoff cycles and optimizes performance.*	*1. Disabled (BIOS & Setup default). 2. Enabled*
Passive Release	*Enabling supports PCI Revision 2.1 latency requirements.*	*1. Enabled (BIOS & Setup default) 2. Disabled*
Delayed Transaction	*Enabling stops the bus from being held to wait states while accessing a slow I/O device.*	*1. Enabled 2. Disabled (BIOS & Setup default)*

Table 4-3: Chipset Features Setup Screen Entry Fields Cont'd

• Power Management Setup Screen

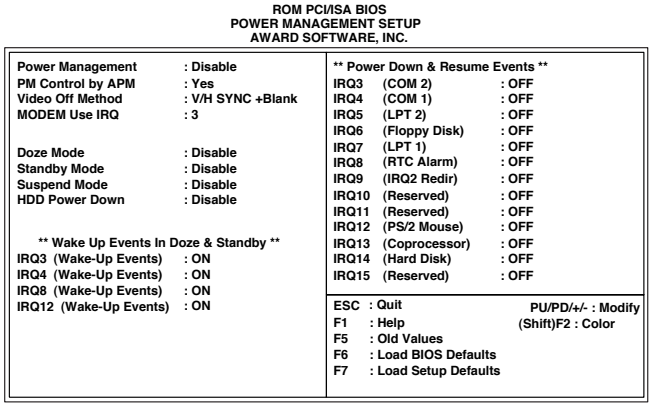


Figure 4-5: Power Management Setup Screen

Explanation

The Power Management Setup screen allows you to configure the system to save energy.

Power Management. The type of power saving selected here is directly related to the four PM Timers: HDD Off After, Doze Mode, Standby Mode, and Suspend Mode. You can choose one of the fixed mode choices or disable it. Min. Power Saving = HDD Off After = 15 min., Doze Mode = 1 hr., Standby Mode = 1 hr., Suspend Mode = 1 min. Max. Power Saving is only available for SL CPUs. HDD Off After = 1 min., Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min. User Defined allows each mode to be set individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Off After which ranges from 1 min. to 15 min. and disable.

PM Timers. The four parameters are Green PC power saving functions that are user configureable when User Defined is selected from the *Power Management* parameter.

PM Events. PM events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from a power saving mode. In effect, the system remains alert for any device configured as Enable, even when the system is in a power down mode.

Entry Fields

Fields	Description	Choices
Power Management	*See Explanation, Page 4-18*	*1. User Define* *2. Disable (BIOS & Setup default).* *3. Min Saving* *4. Max Saving*
PM Control by APM	*Yes to activate Advanced Power Management, enhancing the Max Power Mode.*	*1. No* *2. Yes (BIOS & Setup default).*
Video Off Method	*"Blank Screen" - System only writes blanks to the video buffer. "V/H SYNC+Blank" - System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. "DPMS" - for monitors that support the Display Power Management Signaling standard of the Video Electronics Standards Association (VESA).*	*1. Blank Screen* *2. V/H SYNC+Blank (BIOS & Setup default)* *3. DPMS*
MODEM Use IRQ	*Select the IRQ assigned to the system modem. Activity on the selected IRQ will awaken the system.*	*1. NA* *2. 3 (BIOS & Setup default).* *3. 4* *4. 5* *5. 7* *6. 9* *7. 10* *8. 11*

Table 4-4: Power Management Setup Screen Entry Fields

Fields	Description	Choices
Doze Mode	*When enabled, and after the set time of system inactivity (1 minute to 1 hour), the CPU clock will run at a slower speed while all other devices still operate at full speed. Choices for this mode depend upon the Power Management setting as follows: Min Saving - 1 hour Max Saving - 1 minute This field can only be changed when Power Management is set to "user define."*	*1. Disable (BIOS & Setup default) 2. 1 Min 3. 2 Min 4. 4 Min 5. 6 Min 6. 8 Min 7. 10 Min 8. 20 Min 9. 30Min 10. 40 Min 11. 1 Hour*
Standby Mode	*When enabled, and after the set time of system inactivity (1 minute to 1 hour), the hard drive and the video will shut off while all other devices still operate at full speed. Choices for this mode depend upon the Power Management setting as follows: Min Saving - 1 hour Max Saving - 1 minute This field can only be changed when Power Management is set to "user defined."*	*1. Disable (BIOS & Setup default) 2. 1 Min 3. 2 Min 4. 4 Min 5. 6 Min 6. 8 Min 7. 10 Min 8. 20 Min 9. 30Min 10. 40 Min 11. 1 Hour*

Table 4-4: Power Management Setup Screen Entry Fields Cont'd

Fields	Description	Choices
Suspend Mode	*When enabled, and after the set time of system inactivity (1 minute to 1 hour), all devices except the CPU will shut off. Choices for this mode depend upon the Power Management setting as follows: Min Saving - 1 hour Max Saving - 1 minute This field can only be changed if Power Management is set to "user define."*	*1. Disable (BIOS & Setup default) 2. 1 Min 3. 2 Min 4. 4 Min 5. 6 Min 6. 8 Min 7. 10 Min 8. 20 Min 9. 30Min 10. 40 Min 11. 1 Hour*
HDD Power Down	*When enabled, and after the set time of system inactivity (1 minute to 15 minutes), the hard drive will power down while all other devices remain active. Choices for this mode depend upon the Power Management setting as follows: Min Saving - 15 minutes Max Saving - 1 minute This field can only be changed if Power Management is set to "user define."*	*1. Disable (BIOS & Setup defualt) 2. 1 Min . . . 16. 15 Min in 1 minute increments*

Table 4-4: Power Management Setup Screen Entry Fields Cont'd

Fields	Description	Choices
** Wake Up Events In Doze & Standby **		
IRQ3 (Wake-Up Event) *IRQ4 (Wake-Up Event)* *IRQ8 (Wake-Up Event)* *IRQ12 (Wake-Up Event)*	*Monitoring of four commonly used interrupt requests can be turned ON or OFF so they do not awaken the system for the Doze and Standby modes.* *The default wake-up event is keyboard activity.*	*1. OFF (BIOS default)* *2. ON (Setup default)*
** Power Down & Resume Events **		
IRQ3 (COM 2) *IRQ4 (COM 1)* *IRQ7 (LPT 1)* *IRQ12 (PS/2 Mouse)* *IRQ13 (Coprocessor)* *IRQ14 (Hard Disk)* *IRQ15 (Reserved)*	*Monitoring of common interrupt requests can be turned ON or OFF so they do not awaken the system for the Suspend mode.*	*1. OFF* *2. ON (BIOS & Setup default)*
IRQ5 (LPT2) *IRQ6 (Floppy Disk)* *IRQ8 (RTC Alarm)* *IRQ9 (IRQ2 Redir)* *IRQ10 (Reserved)* *IRQ11 (Reserved)*		*1. OFF (BIOS & Setup default)* *2. ON*

Table 4-4: Power Management Setup Screen Entry Fields Cont'd

- *PNP/PCI Configuration Setup Screen*

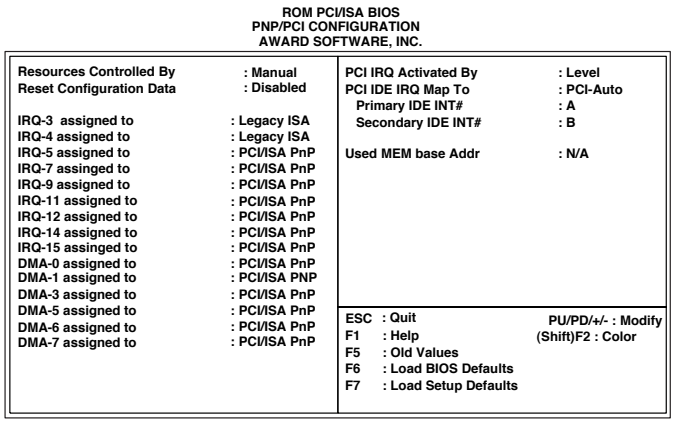


Figure 4-6: PNP/PCI Configuration Setup Screen

Explanation

This screen is for configuring the PCI bus. PCI, or Peripheral Component Interconnect, is a local bus that provides a high-speed data path between the CPU and peripheral devices such as graphic adapters, disk controllers, and network cards.

PnP BIOS Auto-Config. This parameter supports the "Plug and Play" Microsoft/Intel standard for operating systems (Windows® 95) and expansion boards. This feature should only be enabled when using an operating system that supports "Plug and Play."

Entry Fields

Fields	Description	Choices
Resources Controlled By	*Select "Manual" to select IRQ and DMA assignments manually. Select "Auto" to have the BIOS make IRQ and DMA assignments. When "Auto" is selected, all IRQ and DMA fields will disappear.*	*1. Manual (Setup default)* *2. Auto (BIOS defualt)*
Reset Configuration Data	*Normally set to "Disabled." Select "Enabled" to reset Extended System Configuration Data (ESCD) if a newly installed peripheral has caused a conflict that prevents system boot.*	*1. Disabled (BIOS & Setup default)* *2. Enabled*
IRQ-n assigned to	*When resources are controlled manually, each system interrupt must be assigned one of the following types: "Legacy ISA" Devices compliant with the PC AT bus specification. "PCI/ISA PnP" Devices compliant with the Plug and Play standard. These fields are visible and changeable only when Rescources Controlled By is set to "manual" or when the Setup defaults are loaded.*	*1. Legacy ISA (Setup default for IRQ3 and IRQ4)* *2. PCI/ISA PnP (Setup default for IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12 IRQ14 and IRQ15)*
DMA-n assigned to	*When resources are controlled manually, each system DMA channel must be assigned one of the following types: "Legacy ISA" Devices compliant with the PC AT bus specification. "PCI/ISA PnP" Devices compliant with the Plug and Play standard. These fields are visible and changeable only when Rescources Controlled By is set to "manual."*	*1. Legacy ISA* *2. PCI/ISA PnP (Setup default)*

Table 4-5: PNP/PCI Configuration Setup Screen Entry Fields

Fields	Description	Choices
PCI IRQ Activated By	*This parameter selects the method by which the PCI bus acknowledges an IRQ request. Normally set to "Level" unless the assigned PCI device specifies Edge-triggered interrupts.*	*1. Level (BIOS & Setup default)* *2. Edge*
PCI IDE IRQ Map to	*This parameter selects the type of IDE controller (PCI IDE IRQ mapping or PC AT (ISA) interrupts). If ISA is selected, the next two fields (Primary/ Secondary IDE INT#) disappear.*	*1. ISA* *2. PCI-AUTO (BIOS & Setup default)* *3. PCI-SLOT1* *4. PCI-SLOT2* *5. PCI-SLOT3* *6. PCI-SLOT4*
Primary/ Secondary IDE INT#	*Since the PCI IDE interface has two channels, it requires two interrupt services. Standard selection is Primary IDE INT# "A" and Secondary IDE INT# "B."*	*1. A (Primary BIOS & Setup default)* *2. B (Secondary BIOS & Setup default)* *3. C* *4. D*
Used MEM base Addr	*Select a base address for the memory area used by any peripheral that requires high memory. This field cannot be changed by the BIOS. It only appears when the Setup defaults are selected.*	*1. N/A (Setup default)*

Table 4-5: PNP/PCI Configuration Setup Screen Entry Fields Cont'd

• Integrated Peripherals Setup Screen

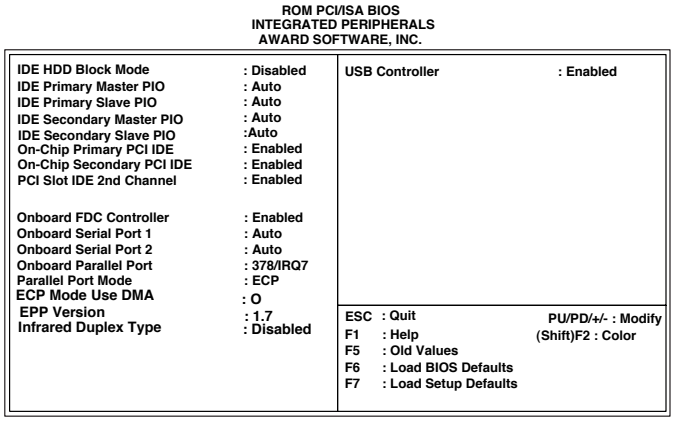


Figure 4-7: Integrated Peripherals Setup Screen

Explanation

This screen allows the user to configure and enable or disable on-board perihperals.

Onboard FDC Controller. This should be enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature.

IDE Primary Master/Slave. This parameter controls the data transfer rate of the IDE drive(s). Selections are from Mode 0 to Mode 4 and AUTO. Mode 0 is the slowest, Mode 4 the fastest. AUTO allows the BIOS to query the drive(s) and select the optimum speed.

Entry Fields

Fields	Description	Choices
IDE HDD Block Mode	*By enabling the block mode for hard drive data transfer, the system can read and write to the drive using large blocks of data instead of individual bytes.*	*1. Disabled (BIOS default)* *2. Enabled (Setup default)*
IDE Primary/ Secondary Master/Slave PIO	*Select the data transfer rate of the primary/secondary master/slave IDE drive. "Auto" allows the BIOS to query the drive(s) and select the optimum speed.*	*1. Auto (BIOS & Setup default)* *2. Mode 0* *3. Mode 1* *4. Mode 2* *5. Mode 3* *6. Mode 4*
On-Chip Primary/ Secondary PCI IDE	*"Enabled" activates the on-board primary IDE interface. Disable if an add-in board is installed in the system*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
PCI Slot IDE 2nd Channel	*Select to disable the second channel on an IDE interface installed in a PCI expansion slot.*	*1. Enabled (BIOS & Setup default)* *2. Disabled*
Onboard FDC Controller	*Select "Enabled" to use the system onboard floppy disk controller. Disable if an FDC board is installed in the system.*	*1. Disabled* *2. Enabled (BIOS & Setup default)*
Onboard Serial Port 1	*Select the IRQ for serial port 1 or disable it.* *COM1=3F8 IRQ4/COM2=2F8 IRQ3* *COM3=2E8 IRQ3/COM4=3E8 IRQ4*	*1. Disabled* *2. COM1/3F8 (Setup default)* *3. COM2/2F8* *4. COM3/3E8* *5. COM4/2E8* *6. Auto (BIOS & Setup default)*
Onboard Serial Port 2	*Select the IRQ for serial port 2 or disable it.* *COM1= 3F8 IRQ4/COM2+2F8* *COM3=2E8 IRQ3/COM4+3E8 IRQ4*	*1. Disabled* *2. COM1/3F8* *3. COM2/2F8* *4. COM3/3E8* *5. COM4/2E8* *6. Auto (BIOS & Setup default)*

Table 4-6: Integrated Peripherals Setup Screen Entry Fields

Fields	Description	Choices
Onboard Parallel Port	Change the default port address of the onboard parallel (printer) port or disable it. 2. = standard LPT1 address 4. = standard LPT2 address 3. = alternate LPT1 address	1. Disabled 2. 378/IRQ7 (BIOS & Setup default) 3. 3BC/IRQ7 4. 278/IRQ5 5. 378/IRQ5
Parallel Port Mode	Select the operational mode of the onboard parallel (printer) port. 1. = Standard parallel port mode. 2. = Extended mode. 3. = Bi-directional mode. 4. = Fast, buffered.	1. Compatible (BIOS & Setup default) 2. Extended 3. EPP 4. ECP
ECP Mode USE DMA	Select the DMA Mode. This field appears and is changeable only when Parallel Port Mode is set to "ECP."	1. 0 2. 1
EPP Version	Select the EPP version. This field appears and is changeable only when Parallel Port Mode is set to "ECP."	1. 1.7 2. 1.9
Infrared Duplex Type	Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-drection transmission. Half-duplex mode permits transmission in one direction only at a time. If no infrared port is present in the system, select "Disabled."	1. Enabled 2. Disabled (BIOS & Setup default)

Table 4-6: Integrated Peripherals Setup Screen Entry Fields Cont'd

- *Password Setting*

When this function is selected, the following message will be displayed at the center of the screen:

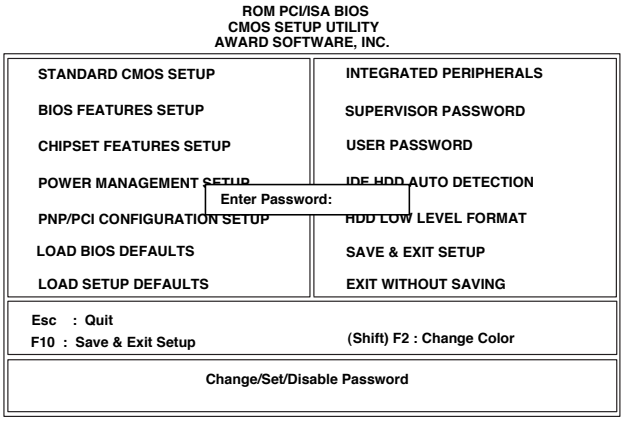


Figure 4-8: Password Setting Screen

Type the password, up to eight characters in length, and press **Enter.** The entered password will clear any previously entered password from CMOS memory. A statement will be displayed requesting confirmation. Type the password again and press **Enter**. To abort this process, press **Esc.**

To disable a password, press **Enter** when prompted to enter the password. The following message will be displayed at the center of the screen:

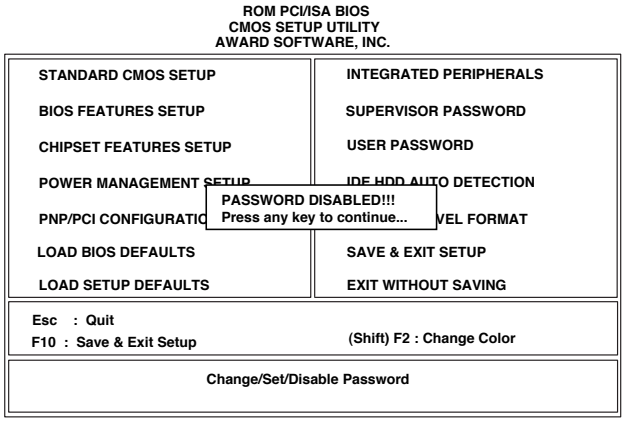


Figure 4-9: Password Disable Screen

Once the password is disabled, the system will boot and Setup can be entered.

When a password has been enabled, it will have to be entered every time Setup is entered. This prevents an unauthorized person from changing any part of the system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to "System," the password will be required both at boot and at entry to Setup. If set to "Setup," prompting only occurs when trying to enter Setup.

- *IDE HDD Auto Detection Setup Screen*

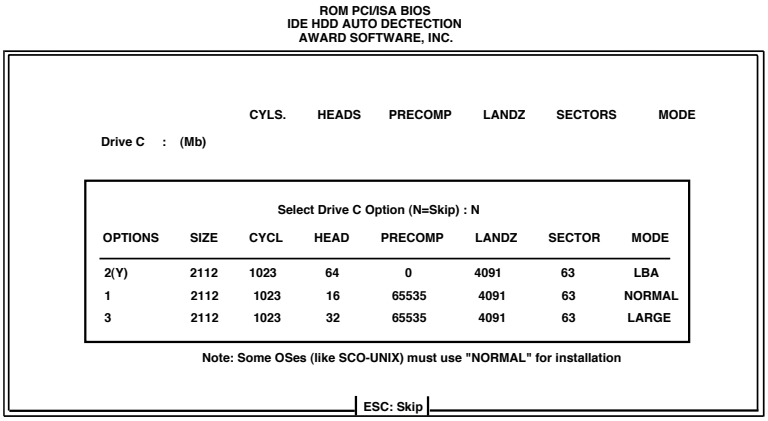


Figure: 4-10: IDE HDD Auto Detection Setup Screen

Explanation

This screen is used for detecting parameters of old or unknown drive geometries. It is only required if standard CMOS setup, set to “Auto” mode, does not detect the drive.

• HDD Low Level Format Setup Screen

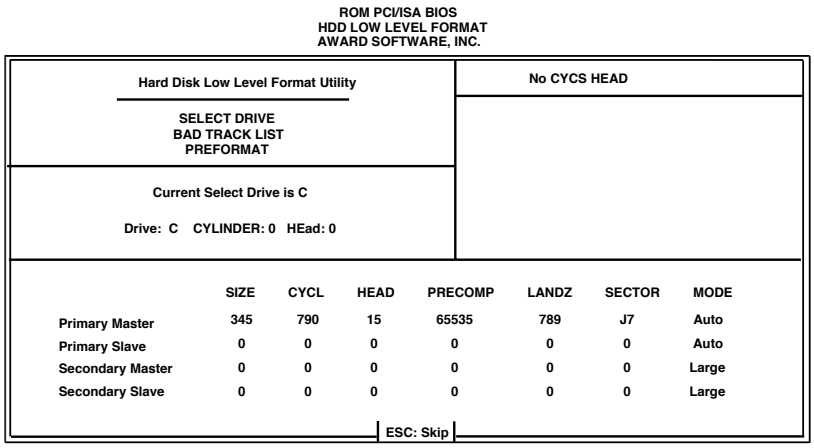


Figure: 4-11: HDD Low Level Format Setup Screen

Explanation

This screen allows the user to low level format the hard drive Its use is not recommended.

Entry Fields

Fields	Description	Choices
Select Drive	*Selects the hard drive.*	*1. Hard drive letters*
Bad Track List	*Allows the user to enter bad track locations on the media.*	*1. Auto Scan Bad Track* *2. Modify Bad Track* *3. Delete Bad Track* *4. Clear Bad Track Table*
Preformat	*Selects parameters of the drive for low level formatting.*	*1. Interleave (1-8)* *2. Autoscan Bad Track (Y or N)* *3. Start (Y or N)*

Table: 4-7: HDD Low Level Format Setup Screen Entry Fields

• POST Messages

During the Power On Self Test (POST), if the BIOS detects an error requiring a fix, it will either sound a beep code or display a message. There is only one beep code in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.

When a POST message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, DEL TO ENTER SETUP

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may be caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE Hard drive cannot be initialized. Make sure the adapter is installed correctly and all cables are correctly and firmly attached. Also make sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DISK CONTROLLER Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT Cannot find or initialize the floppy drive controller. make sure the controller is correctly installed. If there are no floppy drives installed, make sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue to boot.

MEMORY ADDRESS ERROR AT. . . Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY PARITY ERROR AT. . . Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

MEMORY VERIFY ERROR AT. . . Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

OFFENDING ADDRESS NOT FOUND This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

OFFENDING SEGMENT This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

PRESS A KEY TO REBOOT This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT. . . Indicates a parity error in Random Access Memory.

SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT. . . Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

This section contains questions that are most frequently asked of our Customer Support Department about the BIOS setup utility. You may be able to diagnose any difficulty you have by referring to them prior to calling our Customer Support.

Q1 I've made BIOS changes and saved them and now the system won't boot. What can I do?

A A CMOS override can be invoked by pressing the **Insert** key when the computer is rebooted. This resets the system to its defaults.

Q2 Do I have to use the on board IDE or floppy disk controllers?

A No, you may disable them.

Q3 Do you have to use the serial or parallel ports built onto the CPUs?

A No, you may disable them.

Q4 What if you are using a different controller other than the one built into the CPU?

A This is not a problem if you adjust the BIOS to use an off-board controller.

Q5 Can I use a SCSI controller and where should I set the address?

A1 You can use a SCSI controller. You must set the card address for the primary controller in the system. Then find an available appropriate address to set the SCSI BIOS to.

A2 YOU MUST DISABLE THE ON-BOARD IDE CONTROLLER IF YOU WANT THE SCSI CONTROLLER TO BE THE BOOT DEVICE.

Q6 What preventive maintenance steps can I take?

A Ensure all fans in the chassis are working.

Remove and Clean the filter with warm water or com pressed air.

Replace brittle or torn filters.

Allow ample air circulation behind the chassis.

Keep all cables free from tangles.

CAUTION!

Electrostatic discharge (ESD) may damage memory chips, programmed devices, and other electrical components. ESD can be prevented by wearing a wrist strap attached to a groud post on a static mat. Grounding can also be accomplished by touching a chassis that is plugged into a power outlet.

Standard PC-AT I/O Map

Address (Hex)	Device
000 - 01F	DMA Controller
020 - 03F	Interrupt Controller 1
040 - 05F	Timer
060 - 06F	Keyboard Controller
070 - 07F	Real Time Clock (non-maskable interrupt)
080 - 09F	DMA Page Registers
0A0 - 0BF	Interrupt Controller 2
0C0 - 0DF	DMA Controller 2
0F8 - 0FF	Math Co-processor
1F0 - 1FF	Hard Disk Controller
200 - 207	Game I/O
278 - 27F	Prototype Card
2F8 - 2FF	Serial Port 2
300 - 31F	Prototype Card
360 - 36F	(Reserved)
378 - 37F	Parallel Printer Port
380 - 38F	SDLC Bisynchronous 2
3A0 - 3AF	Bisynchronous 1
3B0 - 3BF	Monochrome Display/Printer
3C0 - 3CF	(Reserved)
3D0 - 3DF	Color Graphics Display Adapter
3F0 - 3F7	Floppy Disk
3F8 - 3FF	Serial Port COM1

Table A1-1: Standard PC-AT I/O Map

DMA Channel Page Register and I/O Addresses

Controller 1: 8-bit (ports 000-00F)	
Page Register	**I/O Hex Address**
Channel 0	087
Channel 1	083
Channel 2	081
Channel 3	082
Controller 2: 16-bit (AT Only - ports 0C0-0DF)	
Channel 5	08B
Channel 6	089
Channel 7	08A
Refresh (AT)	08F

Table A1-2: DMA Channel Page Register and I/O Addresses

DMA Channel Assignments

Channel	Function
0	Reserved
1	SDLC
2	Floppy Disk
3	Spare
4	Cascade for CTRL
5	Spare (Reserved)
6	Spare (Reserved)
7	Spare (Reserved)

Table A1-3: DMA Channel Assignments

DMA Controller Register Functions

DMA#		Description
1	2	
000	0C0	CH0 base and current address
001	0C2	CH0 base and current word count
002	0C4	CH1 base and current address
003	0C6	CH1 base and current word count
004	0C8	CH2 base and current address
005	0CA	CH2 base and current word count
006	0CC	CH3 base and current address
007	0CE	CH3 base and current word count
008	0D0	Read status register/write command register
009	0D2	Write request register
00A	0D4	Write single mask register bit
00B	0D6	Write mode register
00C	0D8	Clear byte pointer flip-flop
00D	0DA	Read temporary register/write master clear
00E	0DC	Clear mask register
00F	0DE	Write all mask register bits

Table A1-4: DMA Controller Register Functions

Channel	Name	Function
NMI	NMI	Parity
0	IRQ0	System Timer Output 0*
1	KYBIRQ	Keyboard Output Buffer Full
2	IRQ2	CTRL2 Interrupt (IRQ8 - IRQ15)
3	IRQ3	Serial Port 2 (COM2)
4	IRQ4	Serial Port 1 (COM1)
5	IRQ5	Parallel Port 2
6	IRQ6	Floppy Disk Controller
7	IRQ7	Parallel Port 1
8	RTCIRQ	Real Time Clock
9	IRQ9	Software redirected to INT 0Ah
10	IRQ10	External ISA Bus Device (Reserved)
11	IRQ11	External ISA Bus Device (Reserved)
12	IRQ12	External ISA Bus Device (Reserved)
13	IRQ13	Math Coprocessor
14	IRQ14	Hard Disk Controller
15	IRQ15	External ISA Bus Device (Reserved)

Table A1-5: Interrupts

* These interrupts exist on the system board and are not available on the ISA Bus Connectors.

CMOS RAM Address Map

Address	Description
00 - 0D	*Real Time clock information
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Floppy disk drive type byte - drives A & B
11	Reserved
12	Hard disk type byte - drives C & D
13	Reserved
14	Equipment byte
15	Low base memory size below 1 MB
16	High base memory size below 1 MB
17	Low expansion memory size above 1 MB
18	High expansion memory size above 1 MB
19 - 2D	Reserved
2E - 2F	Checksum for bytes 10 - 2D
30	*Low memory size determined by Pwr Up
31	*High memory size determined by Pwr Up
32	*BCD century byte
33	Information flags (set during power on)
34 - 3F	Reserved

Table A1-6: CMOS RAM Address Map

* These addresses are not verified by CHECKSUM.

Byte	Function	Address
0	Seconds	00
1	Seconds alarm	01
2	Minutes	02
3	Minutes alarm	03
4	Hours	04
5	Hours alarm	05
6	Day of week	06
7	Day of month	07
8	Month	08
9	Year	09
10	Status Register B	0A
11	Status Register C	0B
12	Status Register D	0C
13	Status Register E	0D

Table A1-7: Real-Time Clock Information

ISA Connector Pin Assignments

Pin #	Assign.	Pin #	Assign.	Pin #	Assign.	Pin #	Assign.
A01	IOCHCHK#	B01	GND	C01	SBHE#	D01	EMCS16#
A02	SD7	B02	RESETDRV	C02	LA23	D02	IOCS16#
A03	SD6	B03	+5 V	C03	LA22	D03	IRQ10
A04	SD5	B04	IRQ9	C04	LA21	D04	IRQ11
A05	SD4	B05	+5 V	C05	LA20	D05	IRQ12
A06	SD3	B06	DRQ2	C06	LA19	D06	IRQ15
A07	SD2	B07	-12 V	C07	LA18	D07	IRQ14
A08	SD1	B08	ENDXFR#	C08	LA17	D08	DACK0#
A09	SD0	B09	+12 V	C09	MEMR#	D09	DRQ0
A10	IOCHRDY	B10	GND	C10	MEMW#	D10	DACK5#
A11	AEN	B11	SMEMW#	C11	SD8	D11	DRQ5
A12	SA19	B12	SMEMR#	C12	SD9	D12	DACK6#
A13	SA18	B13	IOW#	C13	SD10	D13	DRQ6
A14	SA17	B14	IOR#	C14	SD11	D14	DACK7#
A15	SA16	B15	DACK3#	C15	SD12	D15	DRQ7
A16	SA15	B16	DRQ3	C16	SD13	D16	+5 V
A17	SA14	B17	DACK1#	C17	SD14	D17	MASTER#
A18	SA13	B18	DRQ1	C18	SD15	D18	GND
A19	SA12	B19	REFRSH#				
A20	SA11	B20	SYSCLK				
A21	SA10	B21	IRQ7				
A22	SA9	B22	IRQ6				
A23	SA8	B23	IRQ5				
A24	SA7	B24	IRQ4				
A25	SA6	B25	IRQ3				
A26	SA5	B26	DACK2#				
A27	SA4	B27	TC				
A28	SA3	B28	BALE				
A29	SA2	B29	+5 V				
A30	SA1	B30	OSC				
A31	SA0	B31	GND				

Table A1-8: ISA Connector Pin Assignments

Pin #	Assign.	Pin #	Assign.	Pin #	Assign.	Pin #	Assign.
A01	TRST#	A32	AD16	B01	-12 V	B32	AD17
A02	+12 V	A33	+3.3 V	B02	TCK	B33	C/BE2#
A03	TMS	A34	FRAME#	B03	GND	B34	GND
A04	TDI	A35	GND	B04	TDO	B35	IRDY#
A05	+5 V	A36	TRDY#	B05	+5 V	B36	+3.3 V
A06	INTA#	A37	GND	B06	+5 V	B37	DEVSEL#
A07	INTC#	A38	STOP#	B07	INTB#	B38	GND
A08	+5 V	A39	+3.3 V	B08	INTD#	B39	LOCK#
A09	CLKC	A40	SDONE	B09	REQ3#	B40	PERR#
A10	+5 V (I/O)	A41	SB0#	B10	REQ1#1	B41	+3.3 V
A11	CLKD	A42	GND	B11	GNT3#	B42	SERR#
A12	GND	A43	PAR	B12	GND	B43	+3.3 V
A13	GND	A44	AD15	B13	GND	B44	C/BE1#
A14	GNT1#	A45	+3.3 V	B14	CLKA	B45	AD14
A15	RST#	A46	AD13	B15	GND	B46	GND
A16	+5 V (I/O)	A47	AD11	B16	CLKB	B47	AD12
A17	GNT0#	A48	GND	B17	GND	B48	AD10
A18	GND	A49	AD09	B18	REQ0#	B49	GND
A19	REQ2#	A50	KEY	B19	+5 V (I/O)	B50	KEY
A20	AD30	A51	KEY	B20	AD31	B51	KEY
A21	+3.3 V	A52	C/BE0#	B21	AD29	B52	AD08
A22	AD28	A53	+3.3 V	B22	GND	B53	AD07
A23	AD26	A54	AD06	B23	AD27	B54	+3.3 V
A24	GND	A55	AD04	B24	AD25	B55	AD05
A25	AD24	A56	GND	B25	+3.3 V	B56	AD03
A26	GNT2#	A57	AD02	B26	C/BE3#	B57	GND
A27	+3.3 V	A58	AD00	B27	AD23	B58	AD01
A28	AD22	A59	+5 V (I/O)	B28	GND	B59	+5 V (I/O)
A29	AD20	A60	REQ64#	B29	AD21	B60	ACK64#
A30	GND	A61	+5 V	B30	AD19	B61	+5 V
A31	AD18	A62	+5 V	B31	+3.3 V	B62	+5 V

Table A1-9: PCI Connector Pin Assignments

Hard Disk Parameter Table

Type	Size (MB)	Cylinders	Heads	Write Precomp	Landing Zone	Sectors/ Track
1	10	306	4	128	305	17
2	21	615	4	300	615	17
3	32	615	6	300	615	17
4	65	940	8	512	940	17
5	49	940	6	512	940	17
6	21	615	4	None	615	17
7	32	462	8	256	511	17
8	31	733	5	None	733	17
9	117	900	15	None	901	17
10	21	820	3	None	820	17
11	37	855	5	None	855	17
12	52	855	7	None	855	17
13	21	306	8	128	319	17
14	44	733	7	None	733	17
16	21	612	4	0	663	17
17	42	977	5	300	977	17
18	59	977	7	None	977	17
19	62	1024	7	512	1023	17
20	31	733	5	300	732	17
21	44	733	7	300	732	17
22	31	733	5	300	733	17
23	10	306	4	0	336	17
24	42	977	5	None	976	17
25	80	1024	9	None	1023	17
26	74	1224	7	None	1223	17
27	117	1224	11	None	1223	17
28	159	1224	15	None	1223	17
29	71	1024	8	None	1023	17
30	98	1024	11	None	1023	17
31	87	918	11	None	1023	17
32	72	925	9	None	926	17
33	89	1024	10	None	1023	17
34	106	1024	12	None	1023	17
35	115	1024	13	None	1023	17
36	124	1024	14	None	1023	17
37	17	1024	2	None	1023	17
38	142	1024	16	None	1023	17
39	119	918	15	None	1023	17
40	42	820	6	None	820	17
41	44	1024	5	None	1023	17
42	68	1024	5	None	1023	26
43	42	809	6	None	852	17
44	64	809	6	None	852	26
45	104	776	8	None	775	33

Note: PRECOMP = 65535 means None!

Table A1-10: Hard Disk Parameters

Appendix 2 Glossary of Terms

B

bidirectional parallel port: An eight-bit port that can be used for an input as well as an output device.

BIOS (Basic Input/Output System): The on-board firmware which communicates with the display, keyboard, printers and other peripheral devices.

bus: A common pathway, or channel, between multiple devices consisting of one or more electrical conductors that transmit power or binary data to the various sections of a computer.

C

cache: A collection of the most recently accessed data or instructions.

CMOS (Complementary Metal Oxide Semiconductor): A technique of using PMOS and NMOS transistors in a complementary fashion where power is consumed only during the switching phase. With the input statically high or low, the power dissipation is essentially zero.

CMOS RAM: Random Access Memory made from CMOS transistors.

D

DMA (Direct Memory Access Channel): A channel for transferring data from host main memory to and from peripherals without direct involvement of the CPU resources.

DRAM (Dynamic Random Access Memory): The main memory in your computer. It needs to be refreshed by a memory controller or it will lose its information.

Appendix 2 Glossary of Terms

E

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power. The information can be erased and new information written.

F

flash BIOS: BIOS that is stored in flash memory rather than in a ROM. Flash BIOS can be upgraded in place, whereas ROM BIOS must be replaced with a newer chip.

Floating Point Unit (FPU): A device which can perform calculations on numbers in floating point format as opposed to simple integers.

I

IDE (Integrated Drive Electronics): A standard of signalling and communicating with a device.

interleave: Multiple banks of memory that overlap to reduce the access time and eliminate wait states.

interrupt: Temporarily halting the operation of a digital computer to respond to (service) an external event.

interval timer: A device that can generate a pulse at a defined interval for background tasks.

IRQ (Interrupt Request): A signal channel used to trigger the CPU to temporarily change tasks.

K

Kilobyte (KB): 1,024 bytes.

N

ns (nano seconds): 1 x 10^{-9} seconds. (There are one billion nanoseconds in one second.)

P

page mode: The ability to read a whole line (page) of memory to reduce access time.

parity: A way to detect corrupted data in DRAM.

parallel port: An eight-bit port usually used for connecting a printer.

PCI (Peripheral Component Interconnect): Local bus for PCs that provides a high-speed data path between the CPU and peripherals (video, disk, network, etc.). The PCI bus coexists in the PC with the ISA or EISA bus. ISA and EISA boards still plug into an ISA or EISA slot, while high-speed PCI controllers plug into a PCI slot. The PCI bus runs at 33MHz, supports 32-bit and 64-bit data paths and bus mastering.

port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

R

RAM (Random Access Memory): The memory used to execute applications while your computer is turned ON. When you turn your computer OFF, all data stored in RAM is lost.

real-time clock (RTC): A CMOS counter used to maintain local time.

retaining bracket: The bracket on the end of the board that attaches to the back of the chassis and contains connectors, usually key board, mouse, serial port, and/or parallel port.

S

serial port: A two channel port, one channel used for "In" transmissions and one for "Out" transmissions.

SCSI (Small Computer System Interface): A high speed, general purpose interface to storage devices.

SRAM (Static Random Access Memory): As opposed to DRAM, this memory does not need to be refreshed by a controller and holds its information as long as the power is on.

T

tag comparator: A memory that tells whether an address is available in the cache.

U

UART (Universal Asynchronous Receiver Transmitter): A circuit that transmits and receives data on the serial port. It converts bytes into serial bits for transmission, and vice versa, and generates and strips the start and stop bits appended to each character.

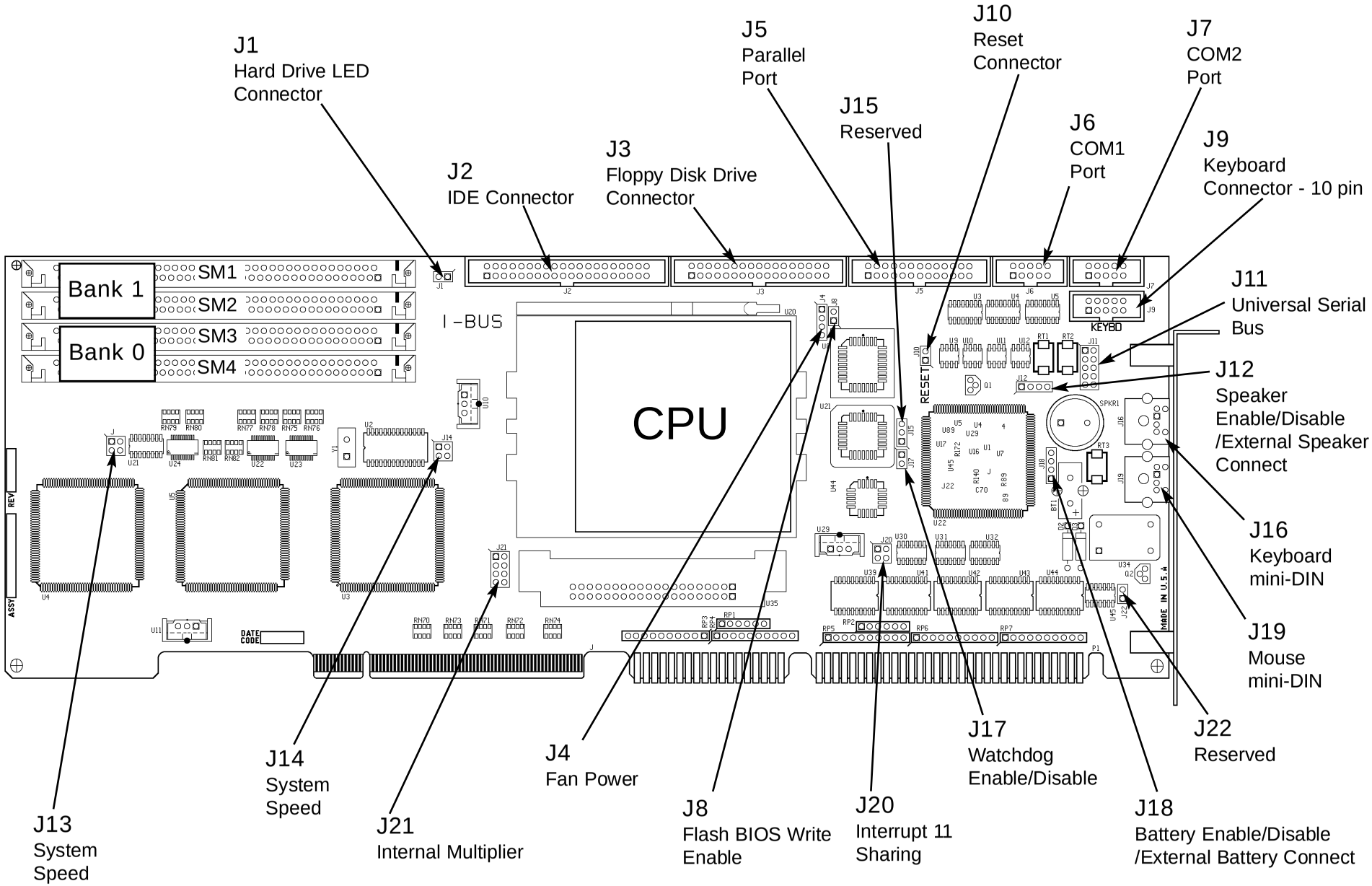
W

wait states: Extra time inserted to allow access to slower devices (e.g. DRAM) or EPROMS.

watchdog timer: A device that watches for CPU inactivity and then resets the CPU after a specified duration of inactivity.

write-back cache: The process where the CPU updates the cache and the DRAM simultaneously but does not wait for the DRAM to complete the update.

write-through cache: The process where the CPU updates the cache and the DRAM simultaneously but the CPU waits for the DRAM to complete the update, resulting in more time being consumed than in write-back.



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Numerics

C

I

J

K

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P